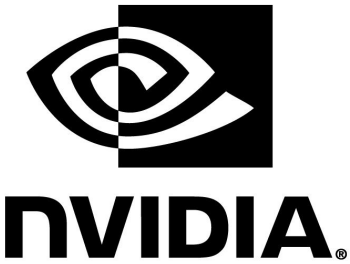
Mobile PCI Express Module Electromechanical Specification

Version 3.1
Revision 1.0

March 1, 2012



Revision History

Rev	Resp	Change
1.0	CF	**Initial Release - Changes from Mobile PCI Express Module Electromechanical Specification Version 3.0 Revision 1.1:** **General** Changed number of RSVD pins from 24 to 14 in pin description (Table 3.13) Clarified module signal integrity specificaton is based on interface specifications, unless explicitly defined (Section 3.5) **Added support for PCIe Gen3 8GT/s** Added PCIe Gen 3 to feature matrix (Table 1.2) Extended connector insertion loss to 12 GHz for PCI-Express Rev 3.0 (Figure 3.1) Extended connector return loss to 12 GHz for PCI-Express Rev 3.0 (Figure 3.2) Extended connector crosstalk to 12 GHz for PCI-Express Rev 3.0 (Figure 3.3) Added 80-85 Ω differential impedance for PCIe 8 GT/s (Table 3.6) Removed PEX_STD_SW# module weak pull-up requirement (Table 3.6) Added PEX_STD_SW# pull-down value reference for 8 GT/s (Table 3.6) Added note to Section 3.4.4 for capacitance requirements for PCIe 8 GT/s Clarified module compliance measurement for PCIe 8 GT/s is at TP2P (Section 3.5.1) Added module PCIe 8 GT/s validation definition (Figure 3.15) Changed description of module behavioral RX to have DFE (Section 3.5.1) Changed behavioral RX to have DFE capability in test setup (Figure 3.15) Clarified system compliance measurement for PCIe 8 GT/s is at TP2P (Section 3.5.2) Added system PCIe 8 GT/s validation definition (Figure 3.18) Added PCIe 8 GT/s module preset requirement (Section 3.5.6) Added PCIe 8 GT/s to module transmitter path eye (Figure 3.29) Added PCIe 8 GT/s system preset requirement (Section 3.5.6) Added PCIe 8 GT/s to system transmitter path eye (Figure 3.30) Added PCIe 8 GT/s system channel classification (Table 3.30) Added DFE state to PCIe 8 GT/s module eye (Figure 3.29) Added DFE state to PCIe 8 GT/s system eye (Figure 3.30) Updated PCIe 8 GT/s module eye height and width (Figure 3.29) Removed PCIe 8 GT/s module eye Dj and Tj (Figure 3.29) Updated PCIe 8 GT/s system transmitter path eye height and width (Figure 3.30) Removed PCIe 8 GT/s system transmitter path eye Dj and Tj (Figure 3.30) Changed PEX_STD_SW# Pull-Down Resistor from 53.6k and 13.3k to 147k and 7.15k for medium channel lengths to allow a binary module input to set low or full swing for 2.5 GT/s and 5 GT/s (Table 3.30) Added separate entries for PCIe RX and PCIe TX in MXM CBB table (Table 3.22) Added eye diagram and table for PCIe Gen3 RX in figure Figure 3.29 Added label TP_SYS to MXM CLB system test point in figures Figure 3.16 and Figure 3.17 Added eye diagram and table for PCIe Gen3 RX in figure Figure 3.30 Specified the Ssystem models for RX cCalibration and the recommended swing settings for Gen1 and Gen2 in table Table 3.30 Changed applicable documents (4.3) to PCIe Base Specification Rev3.0 Changed applicable documents (4.3) to PCIe CEM Specification Rev3.0

Rev	Resp	Change
1.0	CF	**PCIe** Added PCIe Gen 1 to feature matrix (Table 1.2) Added PCIe interface x12 to feature matrix (Table 1.2) Added PCIe REFCLK to feature matrix (Table 1.2) Removed 90 Ω differential impedance for PCIe 2.5-5 GT/s (Table 3.6) Added note for 90 Ω differential impedance for PCIe 2.5-5 GT/s only (Table 3.6) Added PCIe CLB termination (Table 3.23) Added note for PCIe CLB termination location (Table 3.23) **DP** Updated Dual-mode DP Figure 3.7 to use DP specification and TMDS interoperability guide nomenclature for dongle detect signal. Removed non-pre-emphasis voltage ratios (Table 3.25). Same values as DP specificaton. Added support for DP 1.2 HBR2 Added clarification for source of HBR C1 cable model (Section 3.5.1). Clarified module compliance measurement for DP HBR2 is at TP3EQ (Section 3.5.1) Added module DP HBR2 validation definition (Figure 3.14) Clarified DP HBR2 modules must meet TP3EQ (Section 3.5.3) Added HBR2 to module specification (Table 3.25) Changed RBR/HBR non-pre-emphasis ratios in module specification (Table 3.25). Ratio level should be the same value as DP specification. Removed pre-emphasis level 0 minimum in module specification (Table 3.25). Should be the same value as DP specification. Changed pre-emphasis level 0 maximum in module specification (Table 3.25). Should be the same value as DP specification. Changed pre-emphasis delta 1 in module specification (Table 3.25) from 2 to 2.1 dB. Added note for AC common mode noise in module specification (Table 3.25). Set to informative, which aligns with the DP 1.2 specification. Added DP HBR2 eye (Figure 3.19) Added HBR2 to system board specification (Table 3.26) Added DP HBR2 system insertion loss, return loss and PSELFEN (Figure 3.22) Changed applicable documents(4.3) to VESA DP Standard Ver1, Rev2 Changed applicable documents(4.3) to VESA eDP Standard Ver1.2 **Added support for HDMI 1.4** Changed TMDS eye from normalize to absolute voltage (Figure 3.24) for $\leq$ 225MHz pixel clock. To be consistent with HDMI specification. Eye is not different. Only a format change. Updated label of TMDS eye (Figure 3.24) to $\leq$ 225MHz pixel clock Added HDMI eye diagram (Figure 3.25) for > 225MHz pixel clock Updated label for TMDS system insertion and return loss (Figure 3.26) to $\leq$ 225MHz pixel clock Added HDMI system insertion and return loss (Figure 3.27) for >225MHz pixel clock Changed applicable documents (4.3) to HDMI Specification 1.4 **Added support for 6 Display Ports** Changed LVDS interface from required to Optional in display support (Table 1.1) Renamed DVI_HPD to LVDS_L_HPD to support DP_E mapping (Table 3.2 and Table 3.3) Added LVDS_U_HPD to support DP_F mapping (Table 3.2 and Table 3.3) Mapped two DisplayPorts into LVDS function in pin description (Table 3.8) Added DP_E+DP_F to (Table 3.16) Dual-Link DVI mapping Added DP_E and DP_F to (Table 3.17) LVDS multiplexed signal definition Added LVDS_L_HPD and LVDS_U_HPD to (Table 3.17) LVDS multiplexed signal definition Changed DVI_HPD to LVDS_x_HPD (Table 3.14) Added DP_E, DP_F and DP_E+DP_F toTable 3.18 DVI-I DDC mapping

Rev	Resp	Change
1.0	CF	**Added 27MHz Reference Clock** Added Reference Clock to feature matrix (Table 1.2) Added 27MHZ_REF to conector pinout (Table 3.2 and Table 3.3) Added 27MHZ_REF signal pin description (Table 3.12) Added 27MHz reference clock description (Section 3.4.17) Fixed typo in (Table 3.21) to label the reference clock frequency as nominal **Added JTAG** Added JTAG to (Table 1.2) Required and Optional Feature Matrix Added JTAG to connector pinout (Table 3.2 and Table 3.3) Added JTAG to (Table 3.13) Pin Description (System Management Group) Added JTAG specification to applicable documents (4.3) **Increased 3V3 from 1.0A to 2.0A** Added two 3V3 pins to connector pinout (Table 3.2 and Table 3.3) Increased 3V3 current to 2.0A (Table 3.5) **Updated RESET and Power Sequence timing** Changed$T_{PV\text{-}PE}$ from $\geq$ 1 ms to $\geq$ 0 ms(Figure 3.4) Added Reset power down timing and set $T_{FAIL} \leq$ 500 ns (Figure 3.6) **Updated PWR_LEVEL definition** Changed PWR_LEVEL transition requirement from 20% reduction to full reduction (Table 3.11) Changed PWR_LEVEL 0 to 1 transition time from "shall" to "may" (Section 3.4.14) **Added support for Optimized Buffer Flush/Fill (OBFF) and Clarify Wake functionality** Added OBFF to feature matrix (Table 1.2) Added OBFF functionality to WAKE# signal pin description (Table 3.12) Removed WAKE# pull-up voltage requirement in pin description (Table 3.12) Clarified WAKE signal system pull-up voltage (Section 3.4.18) Clarified WAKE assertion only in D3 (Section 3.4.18) Added OBFF functionality to WAKE signal (Section 3.4.18) Clarified 3V3 to be present in states that support wakeup (Section 3.4.18) Added reference to PCIe CEM for WAKE/OBFF AC timing requirement (Section 3.4.18) **Added Module Information Structure** Added MXM MIS SMBus device to Section 3.4.12 Added 0xA0 to Module SMBus Address table to allow MXM MIS with Dual-port I2C ROM (Section 3.4.12) Added 3.4.21 detailing MXM MIS **HDCP** Removed HDCP requirements, Specification will rely on governing specifications for requirements (Section 1.3) Removed HDCP requirements to recommend ASSR with eDP (Section 3.4.6). Content protection is governed by eDP specification. **Mechanical Changes** Changed Form Factor description to accomodate GPUs with heights lower than 1.75 mm (Section 2.1) Clarified that the component heights specified in the tables reflect the actual maximum height of the unsoldered components (Section 2.4) Added W parameter to cooler step height table (Table 4.5) Added offset to cooler steps figure (Figure 4.4) Changed Section 2.3.1 board mounting holes from "plated" to "plated or non-plated"

Contents

List of Figures

List of Tables

Chapter 1

Introduction

The Mobile PCI Express Module (MXM) is a standard graphics interface for PCI Express® systems. This specification describes the electrical, mechanical and thermal interfaces for MXM version 3.1 graphics modules.

The MXM specification is designed for systems that require discrete graphics adapters, but are constrained by limited size, power, and thermal capacity. Typical applications include notebook computers, blade and standard rack mount servers, mobile workstations, and alternative form factor PCs including all-in-one, home theater, and small form factor PCs.

There are two types of MXM version 3.1 modules — Type A and Type B. Each type has a distinct form factor and is targeted for different performance, power and thermal requirements. Figure 1.1 shows various applications where MXM version 3.1 modules are used.

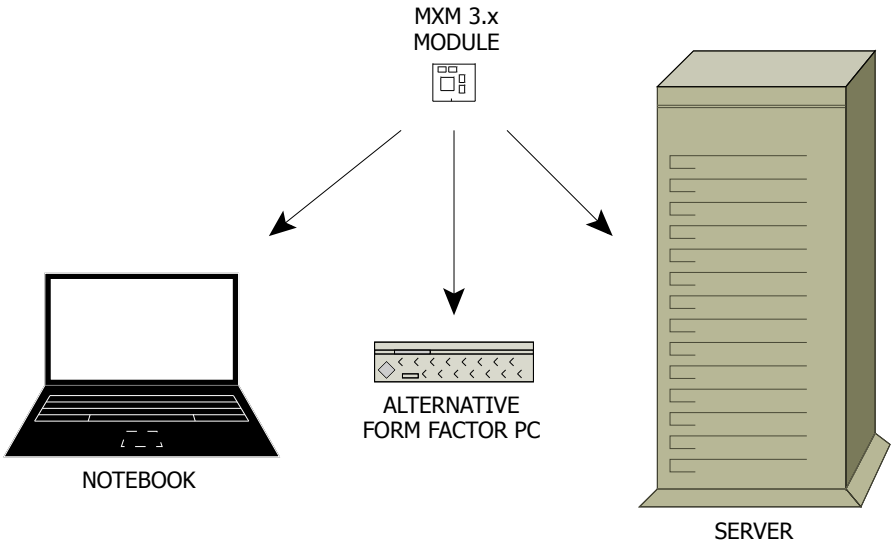


Figure 1.1: MXM Applications

1.1 Background

MXM version 3.x builds upon the experience gained from several years of designing and implementing previous versions of the MXM standard (1.3, 2.0 and 2.1A). While MXM version 3.x is physically similar to previous versions, it is not mechanically or electrically compatible with any of them. The previous MXM devices had limited upgrade capabilities since two incompatible motherboard connectors were used for various MXM board types. The MXM version 3.x specifically addressed this issue by standardizing on a single connector interface with a single pinout for all

MXM device types. The interface connector used with the MXM version 3.x was developed with controlled impedance contacts. While it is the same physical size as the previous 2.x MXM High End version, this connector has almost 25% more signal contacts, which gives the MXM version 3.x devices significantly more capability.

The two current MXM version 3.x module types (A and B) have identical 3D forms where they overlap. The larger of the two modules (Type B) has the same 3D profile as the smaller module (Type A) plus an extension. This was done to provide systems with a wider range of upgradeability, enabling MXM adopters to design a single thermal solution that can be used with all MXM version 3.x modules.

1.2 MXM Version 3.x Benefits

The two form factors defined by the MXM version 3.x specification are electrically, mechanically, and thermally compatible. The thermomechanical compatibility allows the use of Type A modules on Type B systems without any modification to the thermal solution or to the mechanical design of the system. Figure 1.2 shows how the device types can be used in different system designs.

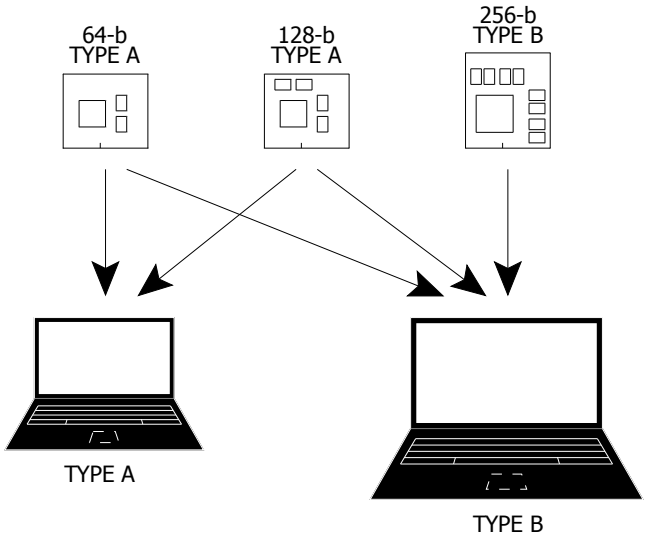


Figure 1.2: MXM Compatibility

MXM version 3.1 supports the following key features:

- Up to 16 lanes PCI Express V3.0
- Up to 8 DDR2, DDR3, GDDR3 or GDDR5 memory devices
- Up to six Dual-mode DisplayPort™ (with support for eDP, DVI and HDMI™)
- Single 24-bit dual-link LVDS, dual-link DVI and HDMI
- Single VGA and TV-out

1.3 Display Support

This specification allows multiple display configurations depending on the board and GPU features. Table 1.1 shows the minimum required set of displays that a module must support. Any other

display is optional on the module. All display outputs are optional on the system (the system is allowed to have no display).

Table 1.1: Required and Optional Display Support

Interface	DP	eDP	HDMI	DVI	DL-DVI	LVDS	VGA	TV
DP_A	required	optional	required	required	N/A	N/A	N/A	N/A
DP_B	optional	optional	optional	optional	N/A	N/A	N/A	N/A
DP_C	required	optional	required	required	N/A	N/A	N/A	N/A
DP_D	optional	optional	optional	optional	N/A	N/A	N/A	N/A
DP_A+DP_B	N/A	N/A	N/A	N/A	optional	N/A	N/A	N/A
DP_A+DP_C	N/A	N/A	N/A	N/A	optional	N/A	N/A	N/A
DP_C+DP_D	N/A	N/A	N/A	N/A	optional	N/A	N/A	N/A
LVDS_L	optional	optional	optional	optional	N/A	optional	N/A	N/A
LVDS_U	optional	optional	optional	optional	N/A	optional	N/A	N/A
LVDS_L+LVDS_U	N/A	N/A	N/A	N/A	optional	optional	N/A	N/A
VGA	N/A	N/A	N/A	N/A	N/A	N/A	required	optional

Note: DisplayPort A and C interfaces are required to be Dual-mode capable. The system designer may choose to provide a Dual-mode connector or level shift the signals on the system board and provide a native DVI or HDMI connector. Refer to Section 3.4.7 for details. Dual-mode support for DisplayPort B and D is optional.

1.4 Required/Optional Feature Matrix

Table 1.2 shows the summary of the features with implementation requirements on both the module and the system. An MXM version 3.1 compliant module must implement all features marked "required" on the module column. A compliant system must implement all features marked "required" in the System column.

Table 1.2: Required and Optional Feature Matrix

Interface/Signal	Description	Module	System
PCIe	PCI Express interface x1	required	required
PCIe	PCI Express Gen 1 (2.5 GT/s)	required	required
PCIe	PCI Express Gen 2 (5 GT/s)	recommended	optional
PCIe	PCI Express Gen 3 (8 GT/s)	recommended	optional
PCIe	PCI Express interface x2, x4, x8, x12, x16	optional	optional
PCIe	PCI Express lane reversal	required	optional
PEX_REFCLK	PCIe reference clock	optional	required
PNL_xxx	Internal flat panel control interface	required	optional
GPIOx	General purpose I/O	required	optional
PWR_LEVEL	Power management interface	required	optional
SMB_xxx	System Management Bus interface	required	optional
TH_OVERT#	Thermal shutdown request	required	required
TH_ALERT#	Thermal interrupt request	optional	optional
TH_PWM	Thermal PWM	optional	optional
PWR_GOOD	Power sequencing sideband	required	optional
PRSNT_x#	MXM module present detect	required	optional
27MHZ_REF	Reference Clock	optional	optional
WAKE#	System wake signal	optional	optional
WAKE#	OBFF function	optional	optional
PWR_EN	Module power enable	required	required
PEX_CLK_REQ#	PCIe clock request	optional	optional
PEX_STD_SW#	PCIe swing control	required	optional
JTAG_xxx	JTAG (IEEE 1149.1)	optional	optional
VGA_DISABLE#	Primary/secondary display select	optional	optional
HDMI_CEC	HDMI 1-wire CEC bus	optional	optional

Chapter 2

Mechanical Specification

This chapter describes the MXM version 3.1 form factors and the associated keep-out zones.

Note: Metric dimensions are the controlling dimension. English equivalents given in brackets may be affected by rounding errors and are provided for reference only.

2.1 Form Factors

The two types of MXM modules have their own form factor and compatible mechanical keep-outs. The keep-outs are necessary for system and thermal solution integration compatibility. The keep-outs are a combination of z-height restrictions and surface keep-outs on the MXM module.

The GPU must be placed on the top side at the center of the four thermal mounting holes (refer to Figure 2.3) to ensure proper load balancing. The minimum GPU height supported by the geometry profile described in Chapter 4 of this specification is 1.75 mm. For any implementation with a GPU height less than 1.75 mm, the GPU manufacturer is to provide an offset value to accommodate a lower-profile part.

The dimensions for each drawing are tabulated in a related table for easier identification. Where a dimension is repeated on another drawing, it is given the same designation as previously used.

Basic dimensions (used for Geometric Dimensioning and Tolerancing) and reference dimensions do not have associated tolerances in the tables. Some reference dimensions are toleranced later in the specification using the same designation while others are obtained from detailed review of the required component.

Note: Tolerances unless otherwise stated are ±0.13 mm [0.005]

2.2 MXM Board Outlines

Figure 2.1 shows the board outlines (top side view) for both Type A and Type B MXM modules.

An additional system keep-out of 0.5 mm [0.020] per side is allowed on the PCB to accommodate whatever means of production panelization is required. This additional clearance is above and beyond the dimensional limits presented here. The location of these features is not specified or controlled.

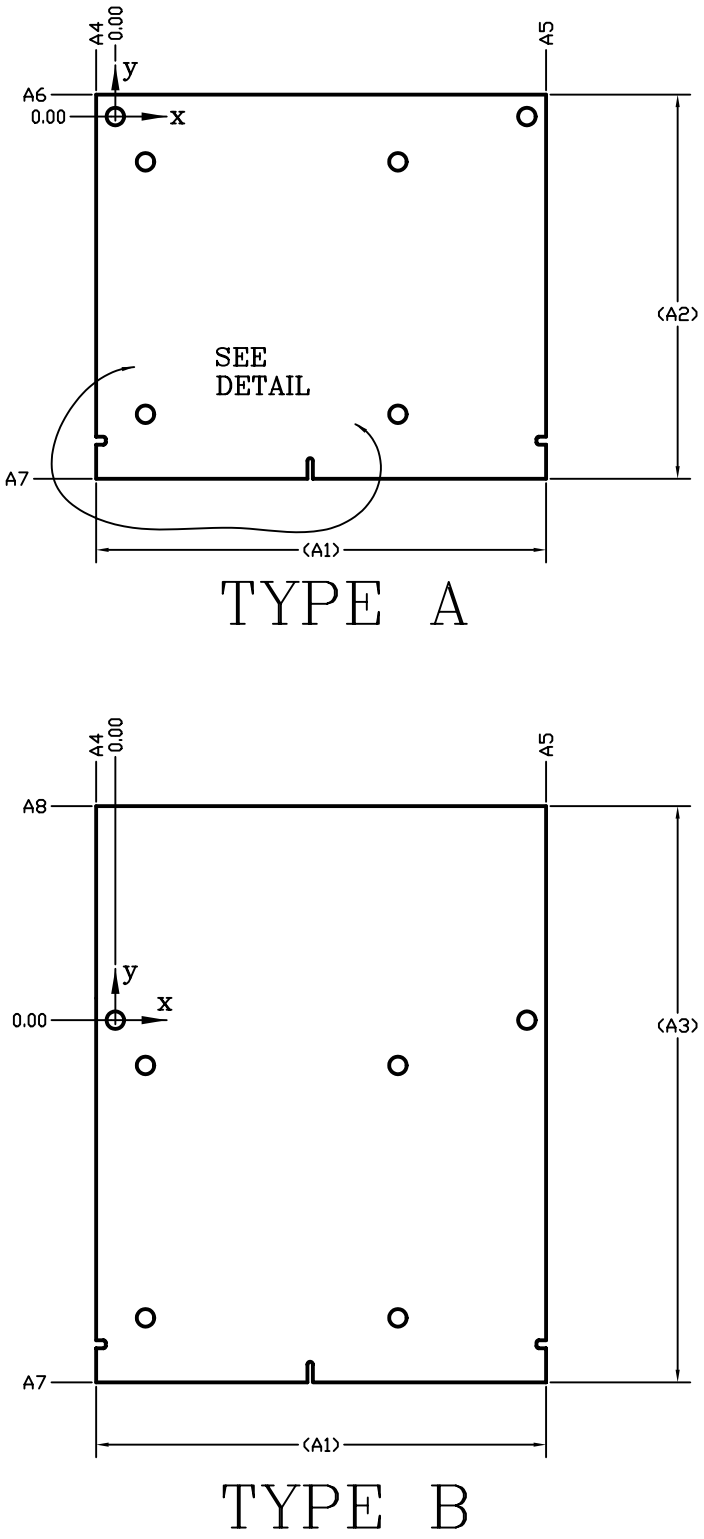


Figure 2.1: Board Outlines

Table 2.1: Board Outline Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
A1		82.00			3.228	
A2		70.00			2.756	
A3		105.00			4.134	
A4	3.37	3.50	3.63	0.133	0.138	0.143
A5	78.37	78.50	78.63	3.085	3.091	3.096
A6	3.87	4.00	4.13	0.152	0.157	0.163
A7	65.87	66.00	66.13	2.593	2.598	2.604
A8	38.87	39.00	39.13	1.530	1.535	1.541

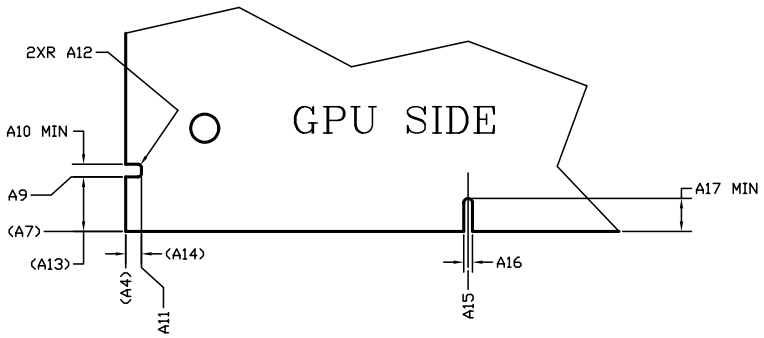


Figure 2.2: Board Slots Detail

Table 2.2: Board Slot Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
A4		3.50			0.138	
A7		66.00			2.598	
A9	59.67	59.80	59.93	2.349	2.354	2.359
A10	1.45			0.057		
A11	1.57	1.70	1.83	0.062	0.067	0.072
A12	0.32	0.50	0.58	0.013	0.020	0.023
A13		6.20			0.244	
A14		1.80			0.071	
A15	35.37	35.50	35.63	1.393	1.398	1.403
A16	0.95	1.00	1.05	0.037	0.039	0.041
A17	3.75			0.148		

2.3 MXM PCB Mounting Holes

All MXM version 3.1 modules have 6 holes. Two are used to secure the board to the system and the other four to fasten the thermal solution to the module.

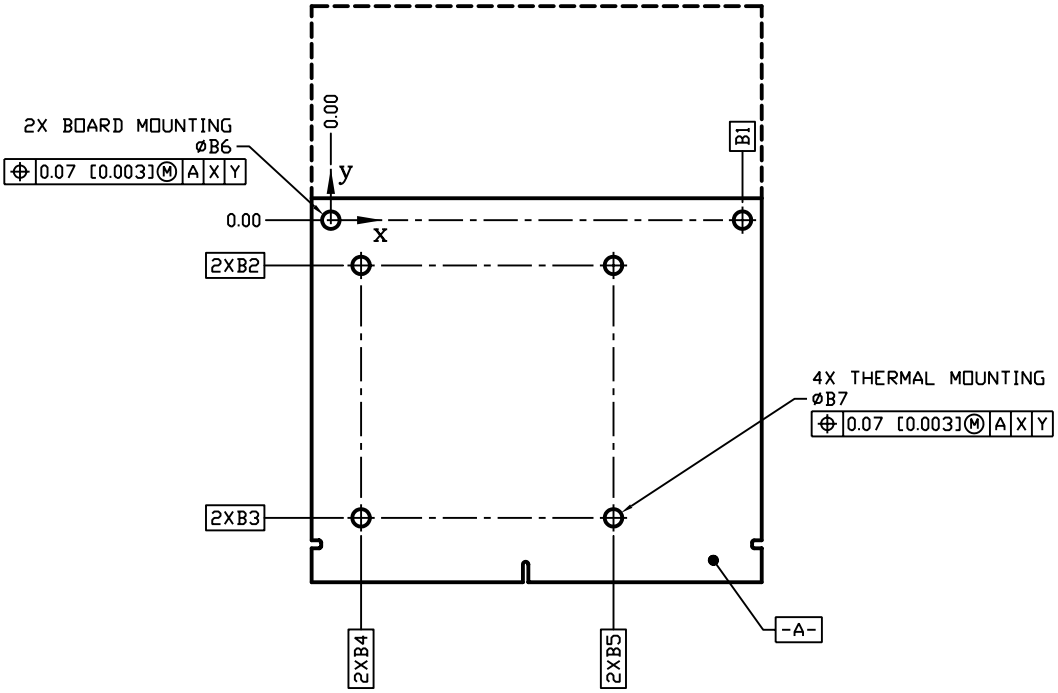


Figure 2.3: Mounting Holes (Type A and Type B)

Table 2.3: Mounting Holes Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
B1		75.00			2.953	
B2		8.25			0.325	
B3		54.25			2.136	
B4		5.50			0.217	
B5		51.50			2.028	
B6	3.07	3.20	3.33	0.121	0.126	0.131
B7	3.07	3.20	3.33	0.121	0.126	0.131

2.3.1 Board Mounting Holes

The two board mounting holes shall be 3.2 mm plated or non-plated holes with 6 mm grounded pad on both the top and bottom sides of the PCB. In case of non-plated holes, the module designer is responsible to ensure good electrical connection between the top and bottom annular ring grounding pads to avoid possible EMI issues.

2.3.2 Thermal Solution Mounting

The four holes surrounding the GPU (which are used for thermal attachment) shall be 3.2 mm plated holes with a 6 mm grounded pad on the top side and a 7 mm grounded pad on the bottom side.

2.3.3 Backing Plate

A system shall provide a backing plate to prevent excessive board warping. The maximum allowed board warpage is measured in accordance with IPC standards (refer to IPC-A-600F). Along the connector edge, this amounts to a maximum displacement of 0.615 mm. The system designer has complete freedom on the design, as long as it stays within the boundaries defined by the specification. Figure 2.4 shows the area that the backing plate is allowed to contact the board.

2.4 Component Height Restrictions

This section contains the component height restrictions for both MXM types. Type A is shown in Figure 2.4 and Figure 2.5. Type B is shown in Figure 2.4 and Figure 2.6.

The keep-out height values defined in this Section represent stand-alone component heights only (absolute max height of the unprocessed/unsoldered component). The thermal solution must provide at least 0.5 mm clearance, under any tolerance conditions, in the x and y direction from the component keepout boundary. Refer to Section 4.2.3 for more details.

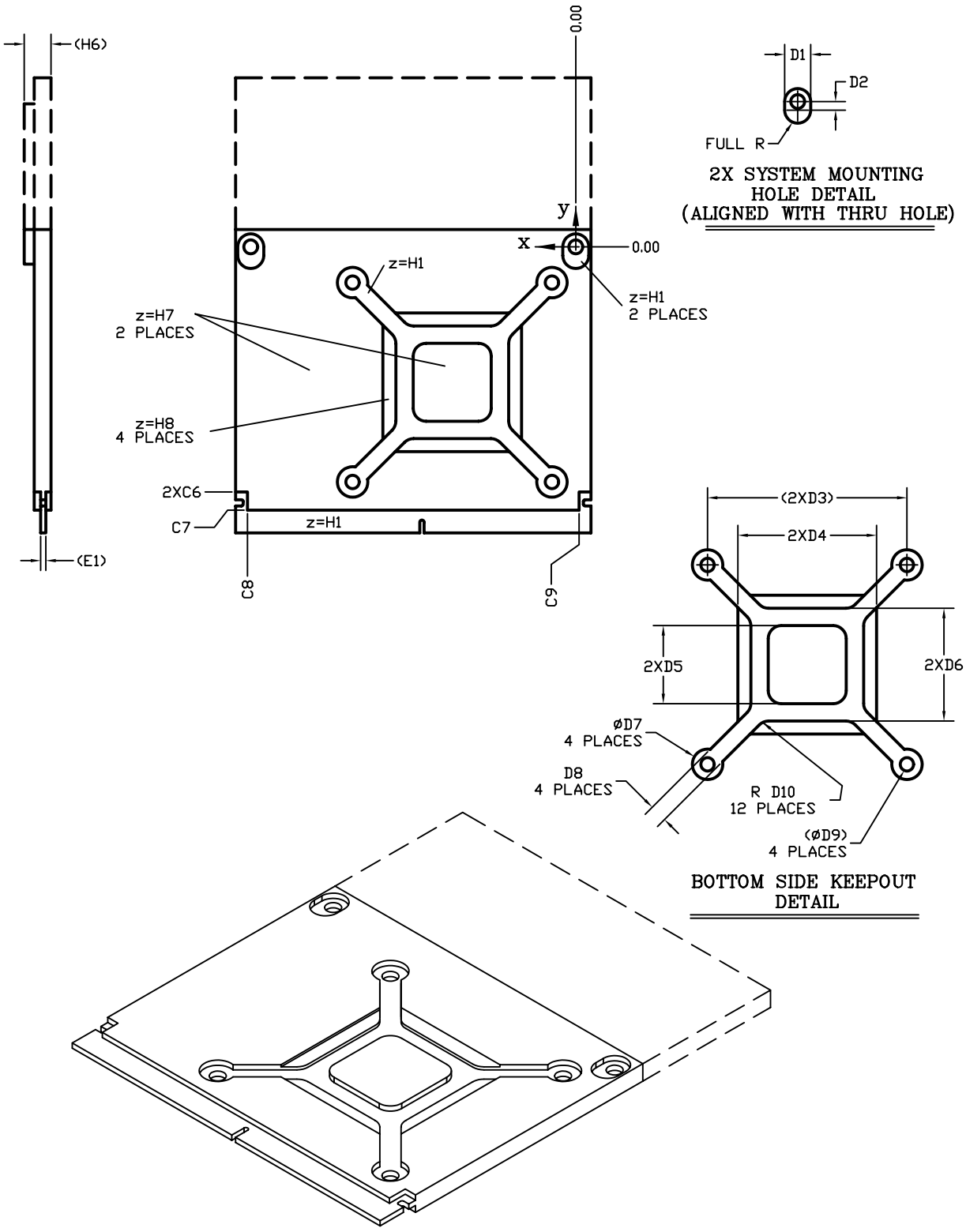


Figure 2.4: Board Bottom Side Height Restrictions (Type A and Type B)

Table 2.4: Board Bottom Side Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
D1		6.00			0.236	
D2		2.00			0.079	
D3		46.00			1.811	
D4		32.00			1.260	
D5		18.00			0.709	
D6		26.00			1.024	
D7		7.00			0.276	
D8		4.00			0.157	
D9		3.20			0.126	
D10		3.00			0.118	
H1			0.00			0.000
H6			6.50			0.256
H7			1.20			0.047
H8			0.70			0.028
C6			56.55			2.226
C7		60.75			2.392	
C8			75.75			2.982
C9			0.75			0.030
E1		1.20			0.047	

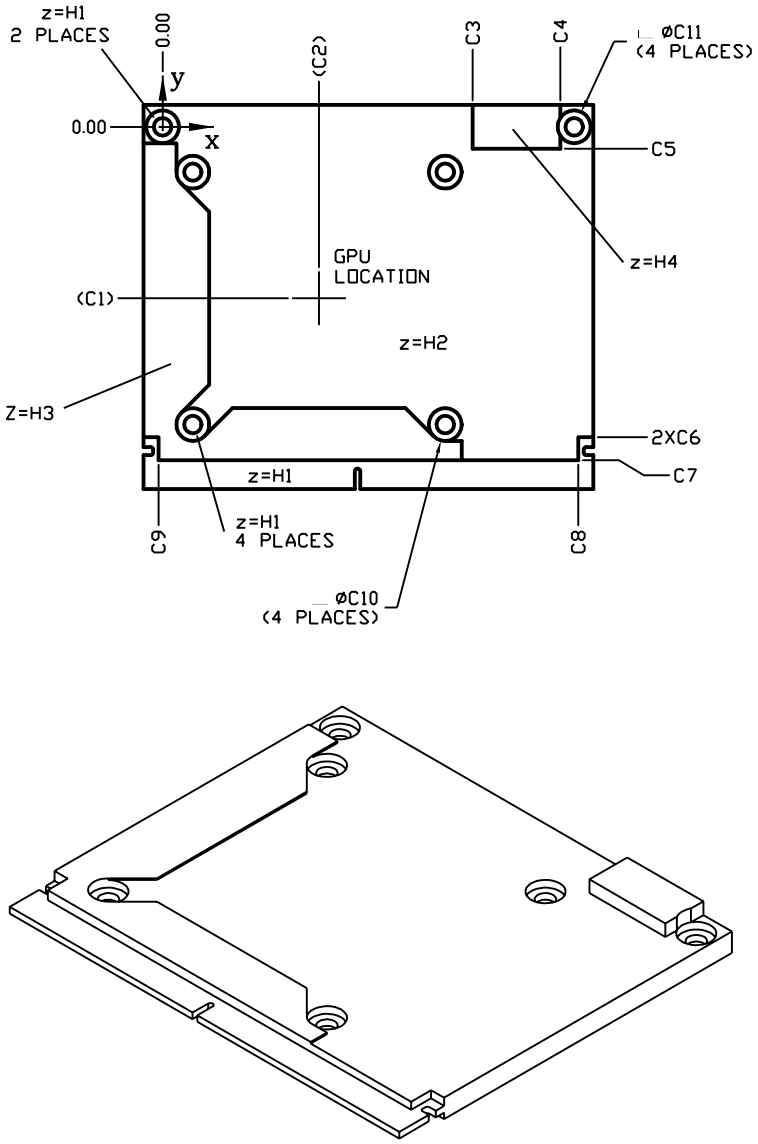


Figure 2.5: Type A Top Side Height Restrictions

Table 2.5: Type A Top Side Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
C1		31.25			1.230	
C2		28.50			1.122	
C3		56.50			2.224	
C4		72.50			2.854	
C5		4.00			0.157	
C6			56.55			2.226
C7		60.75			2.392	
C8			75.75			2.982
C9			0.75			0.030
C10		6.00			0.236	
C11		6.00			0.236	
H1			0.00			0.000
H2			1.50			0.059
H3			1.80			0.071
H4			4.00			0.157

Table 2.6: Type B Top Side Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
C3		56.50			2.224	
C4		72.50			2.854	
C5		4.00			0.157	
C12		14.00			0.551	
C13		33.00			1.299	
C14		2.50			0.098	
C15		28.50			1.122	
C16		46.50			1.831	
H2			1.50			0.059
H4			4.00			0.157
H5			2.20			0.087

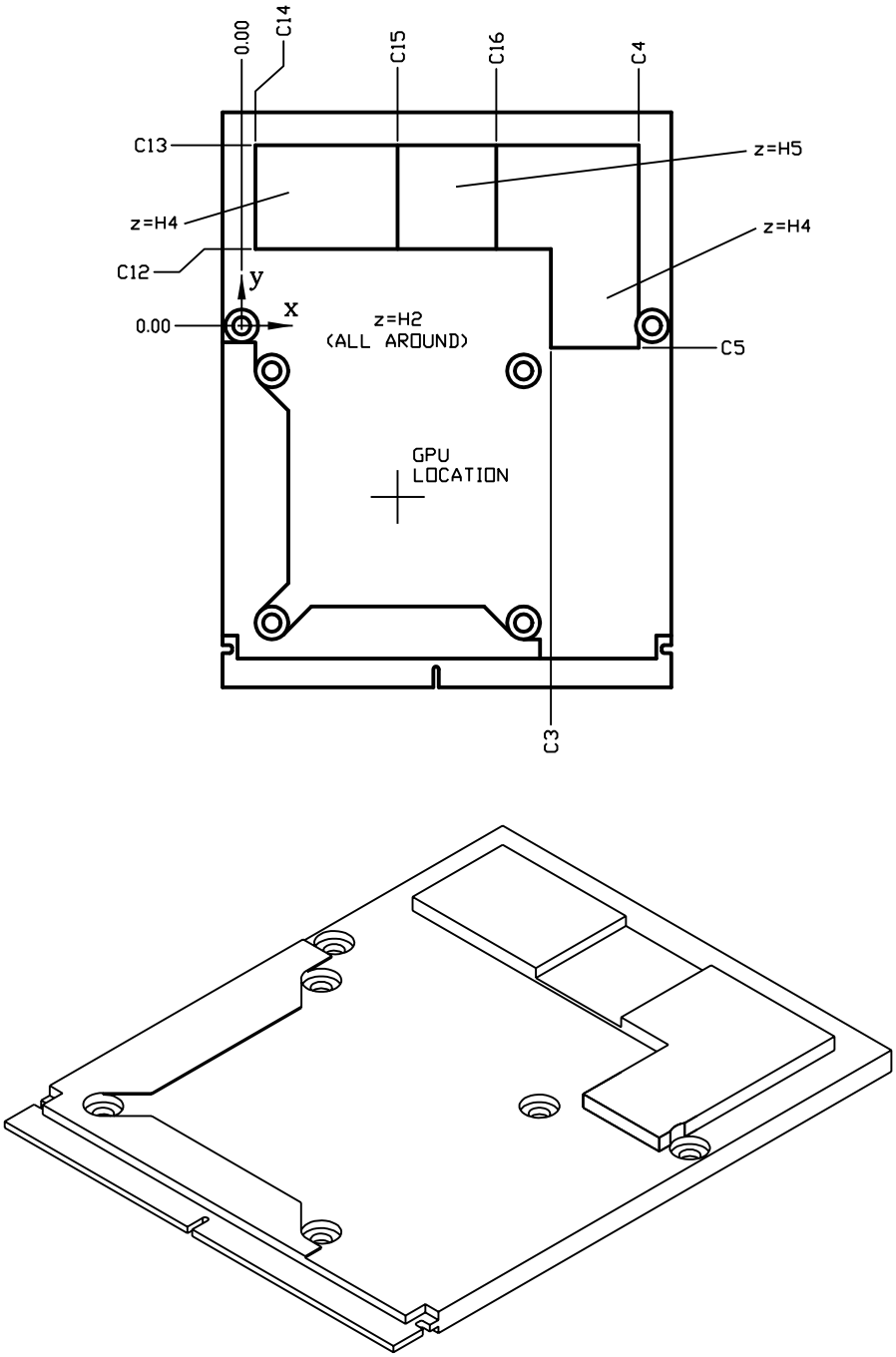


Figure 2.6: Type B Top Side Height Restrictions

2.5 MXM Edge Fingers

MXM utilizes a 0.5 mm pitch, 285-pin, card-edge connection system. Top side contacts on the MXM connector are even numbered (E2, E4, 2, 4, . . .) and bottom side contacts are odd numbered (E1, E3, 1, 3, . . .). The connector accepts an overall PCB thickness of 1.2 mm± 0.1 measured across the fingers including plating and/or metallization. Figure 2.7 shows the board thickness and chamfer requirements.

For good electrical performance, all etch on internal layers under the edge fingers shall be removed. A group of n adjacent power fingers are joined together to allow full pin to finger contact on n-1 pins of that particular group. The module edge finger dimensions are shown in Figure 2.8 through Figure 2.10.

Note: Edge fingers on the module are referenced to the PCB slot center.

PCB flatness with respect to the edge fingers shall not induce undue stress nor cause an open connection between the edge fingers and the connector pin. Any surface defect, including scratches, in the edge finger contact area must not expose bare metal as described in the IPC-A-600F specification.

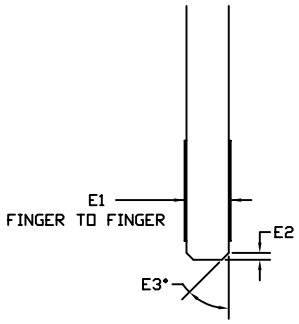


Figure 2.7: Board Thickness and Chamfer

Table 2.7: Board Thickness and Chamfer Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
E1	1.10	1.20	1.30	0.043	0.047	0.051
E2	0.06	0.18	0.30	0.002	0.007	0.012
Symbol	[degrees]			[degrees]		
	min	nom	max	min	nom	max
E3	35	45	55	35	45	55

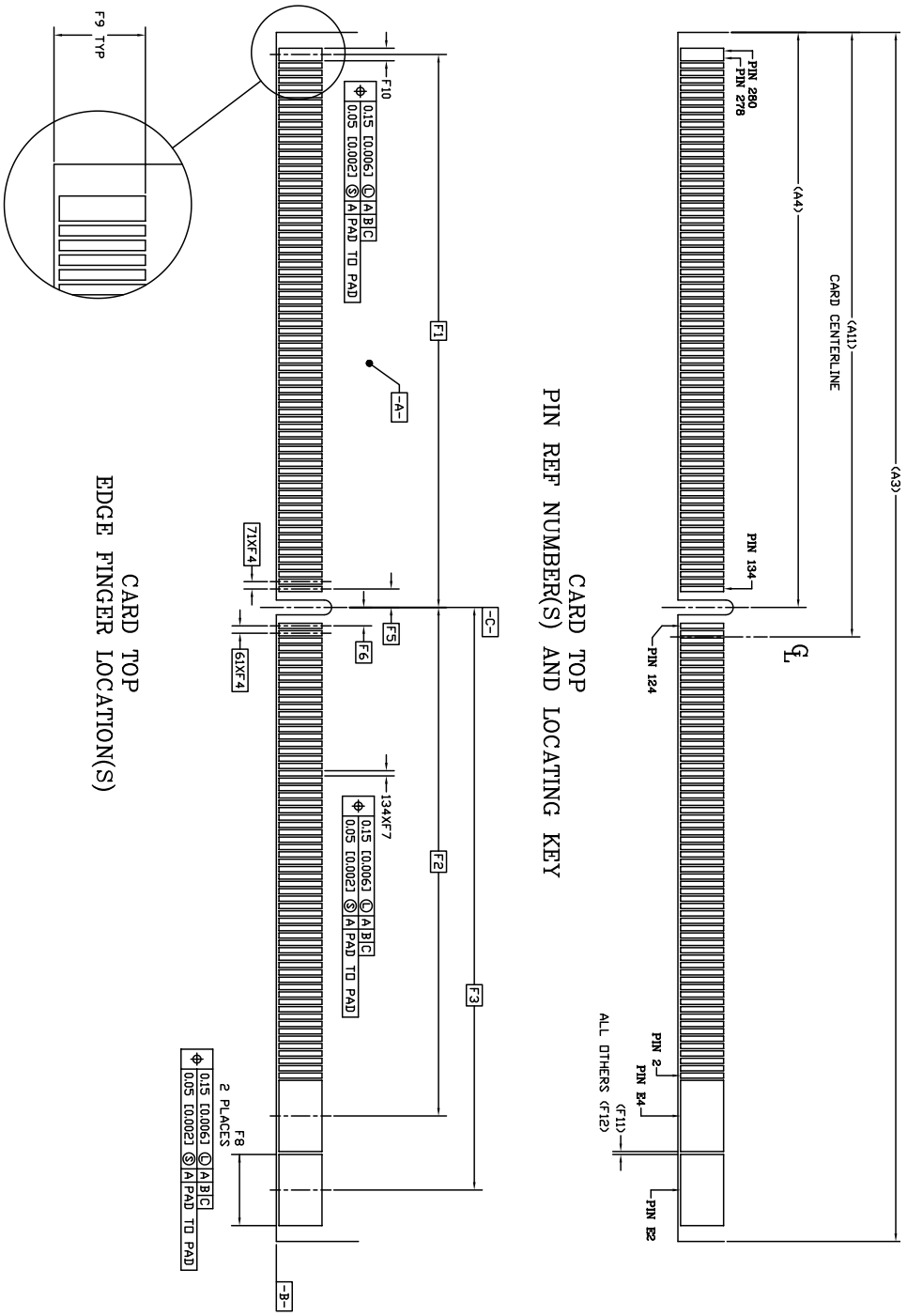


Figure 2.8: Module Edge Finger Top

Table 2.8: Module Edge Finger Top Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
A3		82.00			3.228	
A4		39.00			1.535	
A11		41.00			1.614	
F1		37.50			1.476	
F2		34.49			1.358	
F3		39.51			1.556	
F4		0.50			0.020	
F5		1.25			0.049	
F6		1.25			0.049	
F7	0.32	0.35	0.38	0.013	0.014	0.015
F8	4.79	4.82	4.85	0.189	0.190	0.191
F9	3.02	3.10	3.18	0.119	0.122	0.125
F10	0.82	0.85	0.88	0.032	0.033	0.035
F11		0.20			0.008	
F12		0.15			0.006	

Table 2.9: Module Edge Finger Bottom Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
A4		39.00			1.535	
A11		41.00			1.614	
F4		0.50			0.020	
F7	0.32	0.35	0.38	0.013	0.014	0.015
F8	4.79	4.82	4.85	0.189	0.190	0.191
F9	3.02	3.10	3.18	0.119	0.122	0.125
F11		0.20			0.008	
F12		0.15			0.006	
F13		31.00			1.220	
F14		39.76			1.565	
F15		34.74			1.368	
F16	2.32	2.35	2.38	0.091	0.093	0.094
F17	1.82	1.85	1.88	0.072	0.073	0.074
F18		28.75			1.132	
F19		1.00			0.039	
F20		1.00			0.039	

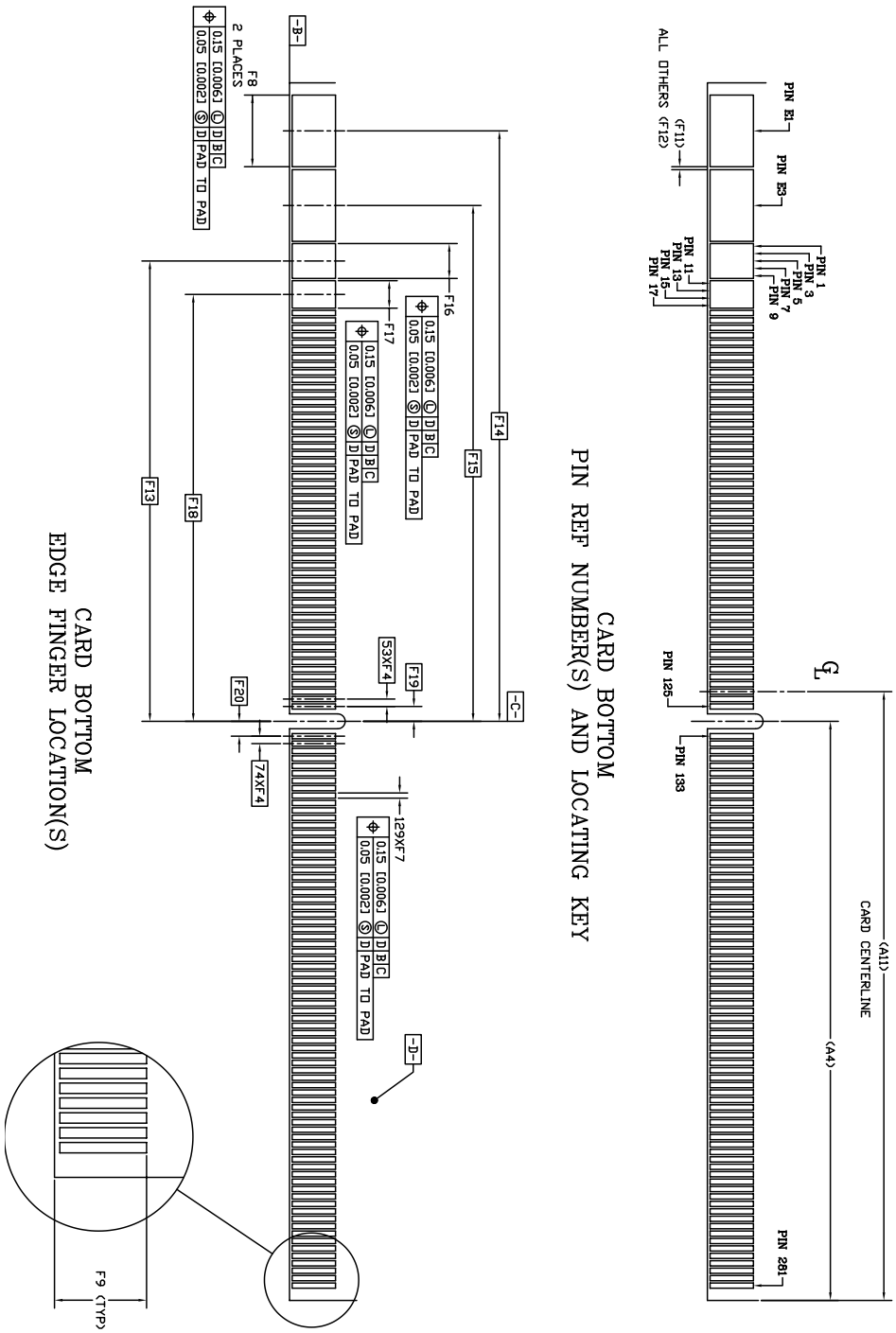


Figure 2.9: Module Edge Finger Bottom

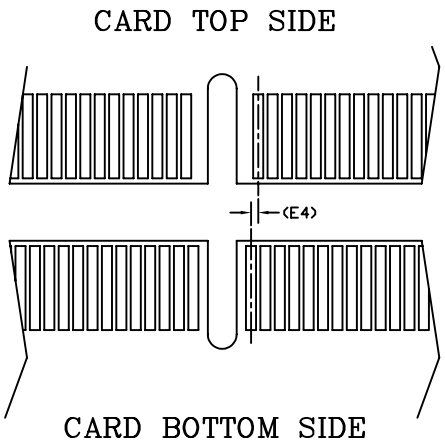


Figure 2.10: Pin Alignment Detail

Table 2.10: Pin Alignment Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
E4		0.25			0.010	

2.6 MXM Connector

It is not the intention of this specification to detail connector contact and housing designs. Each connector vendor may choose to design an MXM connector of various styles as long as the design meets the form, fit and function of the MXM edge fingers (Section 2.5), the module volume definitions (Section 2.4), the electrical performance (Section 3.1) and the mechanical specification contained in this section.

The MXM specification suggests 1.5 mm, 2.7 mm and 5.0 mm connector heights (module to system board). This parameter however can be changed to satisfy custom requirements. Refer to the *MXM Version 3.0 Connector Interoperability Design Guide* for details.

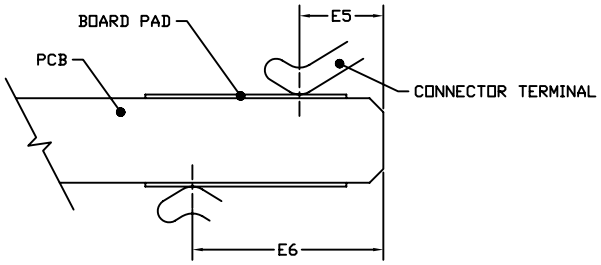


Figure 2.11: Terminal-Board Minimum Engagement

Table 2.11: Terminal-Board Minimum Engagement Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
E5	1.09		2.49	0.043		0.098
E6	1.09		2.49	0.043		0.098

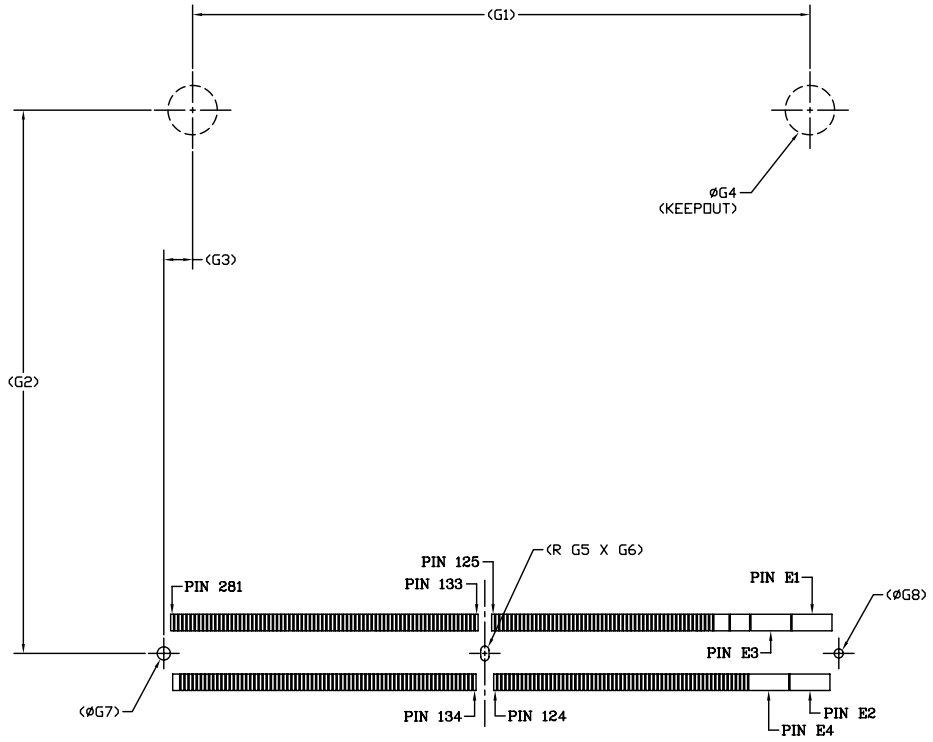


Figure 2.12: Connector Footprint

Table 2.12: Connector Footprint Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
G1		75.00			2.953	
G2		66.00			2.598	
G3		3.50			0.138	
G4	5.87	6.00	6.13	0.231	0.236	0.241
G5		0.50			0.020	
G6		1.80			0.071	
G7		1.60			0.063	
G8		1.10			0.043	

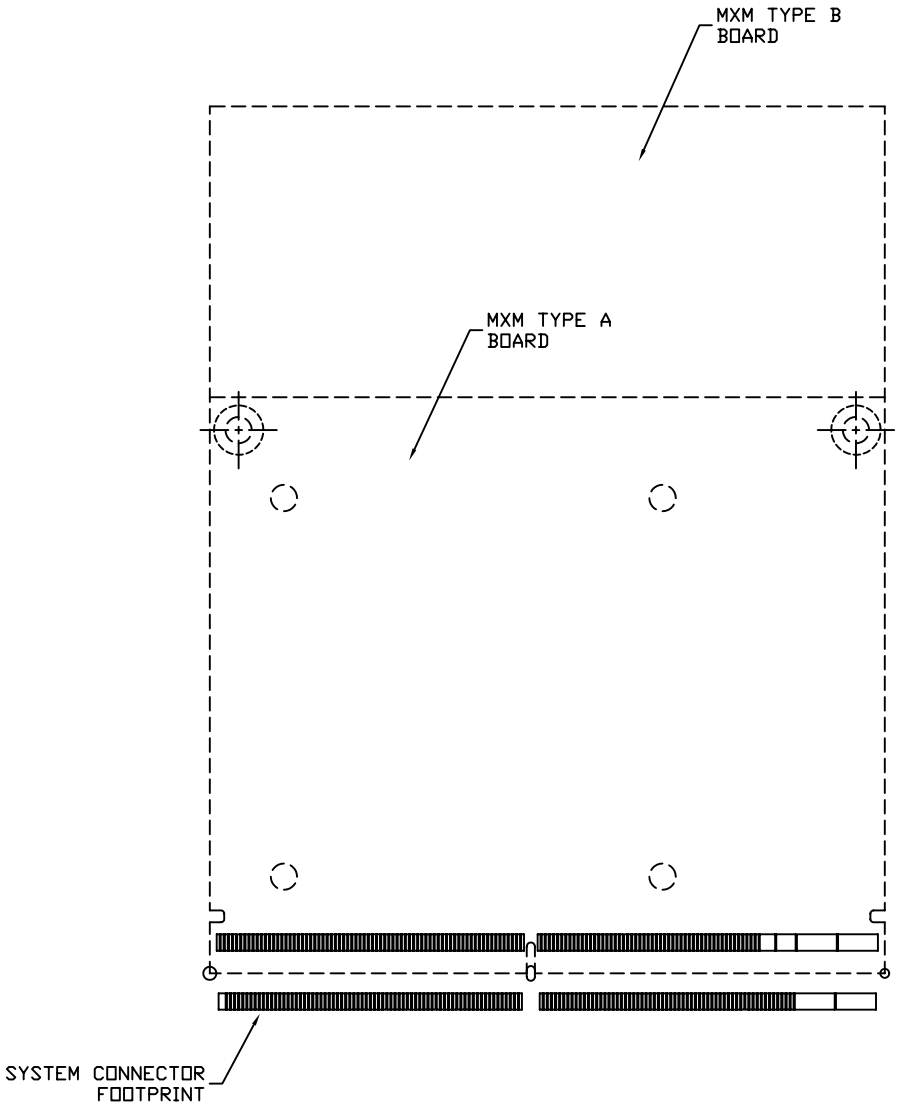


Figure 2.13: Module Location

Table 2.13: Connector Mechanical Performance Requirements

Parameter	**Specification**
Durability	EIA-364-9 30 cycles
Mating and unmating force	EIA-364-13C LIF/angled insertion styled boards: Maximum insertion force: 55 N Maximum extraction force: 60 N Slide-in/side insertion styled boards: Maximum insertion force: 55 N Maximum extraction force: 60 N Note: numbers tabulated using a velocity of 25 mm/min
Vibration	EIA-364-28D – Test condition VII condition D With a 40x40 mm block of 100 grams fastened and centered at the GPU center of a Type B PCB
Shock	EIA-364-27B – Test condition A With a 40x40 mm block of 100 grams fastened and centered at the GPU center of a Type B PCB

Chapter 3

Electrical Specification

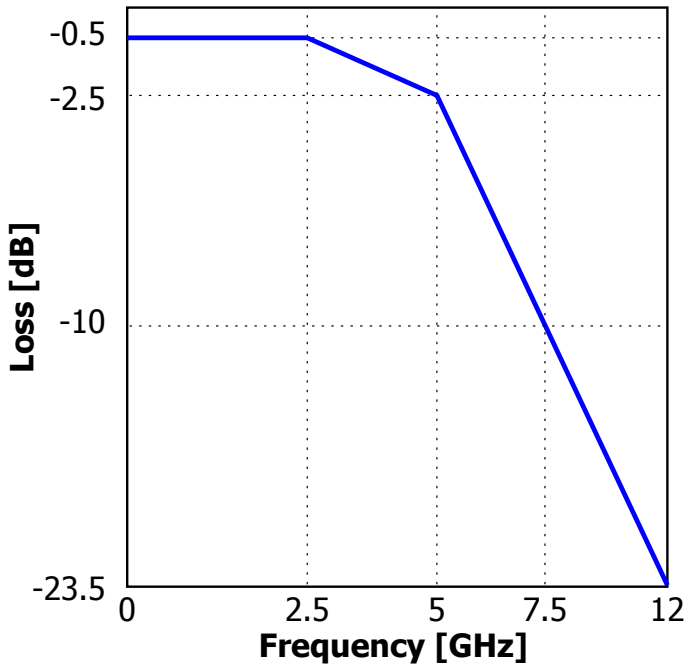
This chapter describes the electrical interface between the MXM module and the host system. All power and I/O signals are routed through the MXM connector down to the motherboard. The motherboard shall connect these signals to the appropriate circuitry depending on the required feature set.

3.1 Connector Electrical Specifications

Table 3.1 lists the electrical requirements for the MXM connector.

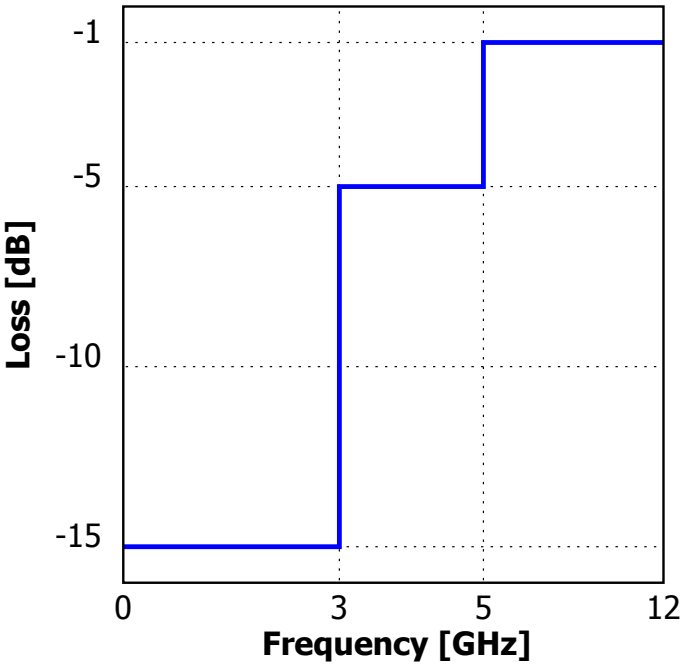
Table 3.1: MXM Connector Electrical Performance Requirements

Parameter	**Specification**
Low Level Contact Resistance	55 mΩ MAX
Insulation Resistance	EIA-364-21C Initial testing 250 MΩ. 50 MΩ after other test procedures
Dielectric Withstanding Voltage	EIA-364-20B – Method B on one pair of upper adjacent contacts and on one pair of lower adjacent contacts. Connector is unmated and unmounted. Barometric pressure at sea level. Apply 0.25 KV AC, (50 Hz) for 1 minute. Current leakage 0.5 mA MAX
Current Rating	0.5 A per pin MIN
Voltage Rating	50 VDC
Differential Impedance	EIA-364-108 85 Ω ± 12.75 at Trise=35 ps
Differential Insertion Loss	EIA-364-101 Refer to Figure 3.1
Differential Return Loss	EIA-364-108 Refer to Figure 3.2
Differential Near End Crosstalk	EIA-364-90 Refer to Figure 3.3



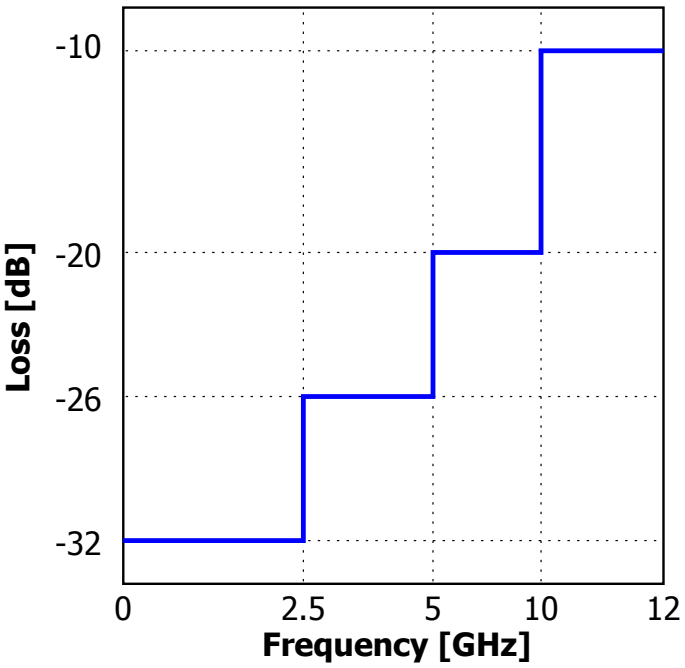
Point	f [GHz]	Loss [dB]
1	0	-0.5
2	2.5	-0.5
3	5.0	-2.5
4	12	-23.5

Figure 3.1: Connector Differential Insertion Loss



Segment	f [GHz]	Loss [dB]
1	0–3	-15
2	3–5	-5
3	5–12	-1

Figure 3.2: Connector Differential Return Loss



Segment	f [GHz]	Loss [dB]
1	0–2.5	-32
2	2.5–5	-26
3	5–10	-20
4	10–12	-10

Figure 3.3: Connector Differential Near End Cross Talk

3.2 Connector Pinout

Table 3.2 and Table 3.3 list the connector pinout.

Table 3.2: Connector Pinout

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
E1	PWR_SRC	E2	PWR_SRC	71	GND	72	PEX_TX11#
E3	GND	E4	GND	73	PEX_RX11#	74	PEX_TX11
1	5V	2	PRSNT_R#	75	PEX_RX11	76	GND
3	5V	4	WAKE#	77	GND	78	PEX_TX10#
5	5V	6	PWR_GOOD	79	PEX_RX10#	80	PEX_TX10
7	5V	8	PWR_EN	81	PEX_RX10	82	GND
9	5V	10	27MHZ_REF	83	GND	84	PEX_TX9#
11	GND	12	GND	85	PEX_RX9#	86	PEX_TX9
13	GND	14	LVDS_U_HPD	87	PEX_RX9	88	GND
15	GND	16	JTAG_TESTEN	89	GND	90	PEX_TX8#
17	GND	18	PWR_LEVEL	91	PEX_RX8#	92	PEX_TX8
19	PEX_STD_SW#	20	TH_OVERT#	93	PEX_RX8	94	GND
21	VGA_DISABLE#	22	TH_ALERT#	95	GND	96	PEX_TX7#
23	PNL_PWR_EN	24	TH_PWM	97	PEX_RX7#	98	PEX_TX7
25	PNL_BL_EN	26	GPIO0	99	PEX_RX7	100	GND
27	PNL_BL_PWM	28	GPIO1	101	GND	102	PEX_TX6#
29	HDMI_CEC	30	GPIO2	103	PEX_RX6#	104	PEX_TX6
31	LVDS_L_HPD	32	SMB_DAT	105	PEX_RX6	106	GND
33	LVDS_DDC_DAT	34	SMB_CLK	107	GND	108	PEX_TX5#
35	LVDS_DDC_CLK	36	GND	109	PEX_RX5#	110	PEX_TX5
37	GND	38	OEM0	111	PEX_RX5	112	GND
39	OEM1	40	OEM2	113	GND	114	PEX_TX4#
41	OEM3	42	OEM4	115	PEX_RX4#	116	PEX_TX4
43	OEM5	44	OEM6	117	PEX_RX4	118	GND
45	OEM7	46	GND	119	GND	120	PEX_TX3#
47	GND	48	PEX_TX15#	121	PEX_RX3#	122	PEX_TX3
49	PEX_RX15#	50	PEX_TX15	123	PEX_RX3	124	GND
51	PEX_RX15	52	GND	125	GND	126	KEY
53	GND	54	PEX_TX14#	127	KEY	128	KEY
55	PEX_RX14#	56	PEX_TX14	129	KEY	130	KEY
57	PEX_RX14	58	GND	131	KEY	132	KEY
59	GND	60	PEX_TX13#	133	GND	134	GND
61	PEX_RX13#	62	PEX_TX13	135	PEX_RX2#	136	PEX_TX2#
63	PEX_RX13	64	GND	137	PEX_RX2	138	PEX_TX2
65	GND	66	PEX_TX12#	139	GND	140	GND
67	PEX_RX12#	68	PEX_TX12	141	PEX_RX1#	142	PEX_TX1#
69	PEX_RX12	70	GND	143	PEX_RX1	144	PEX_TX1

Table 3.3: Connector Pinout (continued)

Pin	Signal Name	Pin	Signal Name
145	GND	146	GND
147	PEX_RX0#	148	PEX_TX0#
149	PEX_RX0	150	PEX_TX0
151	GND	152	GND
153	PEX_REFCLK#	154	PEX_CLK_REQ#
155	PEX_REFCLK	156	PEX_RST#
157	GND	158	VGA_DDC_DAT
159	JTAG_TDO	160	VGA_DDC_CLK
161	JTAG_TDI	162	VGA_VSYNC
163	JTAG_TCLK	164	VGA_HSYNC
165	JTAG_TMS	166	GND
167	JTAG_TRST#	168	VGA_RED
169	LVDS_UCLK#	170	VGA_GREEN
171	LVDS_UCLK	172	VGA_BLUE
173	GND	174	GND
175	LVDS_UTX3#	176	LVDS_LCLK#
177	LVDS_UTX3	178	LVDS_LCLK
179	GND	180	GND
181	LVDS_UTX2#	182	LVDS_LTX3#
183	LVDS_UTX2	184	LVDS_LTX3
185	GND	186	GND
187	LVDS_UTX1#	188	LVDS_LTX2#
189	LVDS_UTX1	190	LVDS_LTX2
191	GND	192	GND
193	LVDS_UTX0#	194	LVDS_LTX1#
195	LVDS_UTX0	196	LVDS_LTX1
197	GND	198	GND
199	DP_C_L0#	200	LVDS_LTX0#
201	DP_C_L0	202	LVDS_LTX0
203	GND	204	GND
205	DP_C_L1#	206	DP_D_L0#
207	DP_C_L1	208	DP_D_L0
209	GND	210	GND
211	DP_C_L2#	212	DP_D_L1#
213	DP_C_L2	214	DP_D_L1

Pin	Signal Name	Pin	Signal Name
215	GND	216	GND
217	DP_C_L3#	218	DP_D_L2#
219	DP_C_L3	220	DP_D_L2
221	GND	222	GND
223	DP_C_AUX#	224	DP_D_L3#
225	DP_C_AUX	226	DP_D_L3
227	RSVD	228	GND
229	RSVD	230	DP_D_AUX#
231	RSVD	232	DP_D_AUX
233	RSVD	234	DP_C_HPD
235	RSVD	236	DP_D_HPD
237	RSVD	238	RSVD
239	RSVD	240	3V3
241	RSVD	242	3V3
243	RSVD	244	GND
245	RSVD	246	DP_B_L0#
247	RSVD	248	DP_B_L0
249	RSVD	250	GND
251	GND	252	DP_B_L1#
253	DP_A_L0#	254	DP_B_L1
255	DP_A_L0	256	GND
257	GND	258	DP_B_L2#
259	DP_A_L1#	260	DP_B_L2
261	DP_A_L1	262	GND
263	GND	264	DP_B_L3#
265	DP_A_L2#	266	DP_B_L3
267	DP_A_L2	268	GND
269	GND	270	DP_B_AUX#
271	DP_A_L3#	272	DP_B_AUX
273	DP_A_L3	274	DP_B_HPD
275	GND	276	DP_A_HPD
277	DP_A_AUX#	278	3V3
279	DP_A_AUX	280	3V3
281	PRSNT_L#	-	-

3.3 Pin Description

This section contains pin descriptions for all signals divided in logical/functional groups. For each signal an input/output classification, a signal type and, when meaningful, a PCB trace impedance are provided. The input/output classification is always relative to the MXM graphics module. Table 3.4 describes all the signal types used in the next sections. Impedance is specified as single ended (SE), differential (diff) or not impedance controlled according to the type of signal.

Table 3.4: Signal Types

Type	Description
Power	Power rail
Diff	Low voltage differential signal (PCIe, LVDS, TMDS or DP)
CMOS	3.3 V push pull CMOS signal
OD	3.3 V open drain signal
Analog	Low voltage analog signal

Note: All impedance controlled signals mentioned in this chapter are assumed to have a ±10% tolerance unless specified explicitly.

3.3.1 Power Group

Table 3.5 shows the MXM module power requirements. The voltage tolerances in the table are specified as measured on the module edge finger. The system must be able to supply the full specified current on all rails (except PWR_SRC) at all times. The current capability of the PWR_SRC rail must be defined by the system in the MXM system information structure. Refer to the *MXM Graphics Module Software Specification* for details.

Table 3.5: MXM Power Rails

Signal Name	I/O	Type	Impedance	Voltage	Current
PWR_SRC	I	Power	N/A	7–20 V	up to 10 A
5V	I	Power	N/A	5.0 V ± 6%	2.5 A
3V3	I	Power	N/A	3.3 V ± 6%	2.0 A

Note: PWR_SRC voltage range is assumed to be DC or RMS. However under any circumstances the maximum peak voltage shall not exceed 22 V and the minimum voltage shall not fall below 6.5 V.

3.3.2 PCI Express Signal Group

The MXM version 3.1 supports PCI Express interconnect up to sixteen lanes. It is compliant with the *PCI Express Base Specification* revision 3.0 or earlier except for power delivery and power management. MXM power requirements supersede PCI Express power specifications. Table 3.6 shows the list of signals for the PCIe group

Table 3.6: Pin Description (PCIe group)

Signal Name	I/O	Type	Impedance	Description
PEX_TXxx PEX_TXxx#	I	Diff	80-85 Ω diff	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board.
PEX_RXxx PEX_RXxx#	O	Diff	80-85 Ω diff	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.
PEX_REFCLK PEX_REFCLK#	I	Diff	90 Ω diff	PCI Express reference clock.
PEX_RST#	I	CMOS	N/A	PCI Express reset signal.
PEX_CLK_REQ#	O	OD	N/A	PCI Express clock request. Pull-up resistor to 3.3 V is required on the system board if the function is supported. If the GPU does not support the feature the pin must be connected to GND on the module.
PEX_STD_SW#	I	OD	N/A	PCI Express swing select pin. Module will default to low swing level if the pin is no connect on the system board. Must be tied to GND on the system board to select full swing level. System that supports 8 GT/s must have a pull-down resistor to GND on the system board. Refer to Table 3.30 for pull-down resistor value.

Note: Systems or Modules that support 2.5 GT/s and/or 5 GT/s only may use 90 differential impedance for PEX_TXxx and PEX_RXxx.

3.3.3 DisplayPort Signal Group

The DisplayPort signal group provides the interface for connecting up to four digital displays. Compliant modules are required to support at least port A and port C. Support for the other ports is optional.

Table 3.7: Pin Description (DP group)

Signal Name	I/O	Type	Impedance	Description
DP_A_Lx DP_A_Lx#	O	Diff	90 Ω diff	Dual-mode DisplayPort A. DC blocking caps must be placed on the system board.
DP_A_AUX DP_A_AUX#	I/O	Diff / OD	90 Ω diff	DisplayPort A auxiliary channel/DDC. DC blocking caps must be placed on the system board. Refer to Section 3.4.5 for Dual-mode support.
DP_A_HPD	I	CMOS	N/A	DisplayPort A hot plug detect. 100 KΩ pull-down required on module. Protection circuitry must be placed on the system board.
DP_B_Lx DP_B_Lx#	O	Diff	90 Ω diff	DisplayPort B. DC blocking caps must be placed on the system board. Dual-mode support is optional.
DP_B_AUX DP_B_AUX#	I/O	Diff / OD	90 Ω diff	DisplayPort B auxiliary channel/optional DDC. DC blocking caps must be placed on the system board.
DP_B_HPD	I	CMOS	N/A	DisplayPort B hot plug detect. 100 KΩ pull-down required on module. Protection circuitry must be placed on the system board.
DP_C_Lx DP_C_Lx#	O	Diff	90 Ω diff	Dual-mode DisplayPort C. DC blocking caps must be placed on the system board.
DP_C_AUX DP_C_AUX#	I/O	Diff / OD	90 Ω diff	DisplayPort C auxiliary channel/DDC. DC blocking caps must be placed on the system board. Refer to Section 3.4.5 for Dual-mode support.
DP_C_HPD	I	CMOS	N/A	DisplayPort C hot plug detect. 100 KΩ pull-down required on module. Protection circuitry must be placed on the system board.
DP_D_Lx DP_D_Lx#	O	Diff	90 Ω diff	DisplayPort D. DC blocking caps must be placed on the system board. Dual-mode support is optional.
DP_D_AUX DP_D_AUX#	I/O	Diff / OD	90 Ω diff	DisplayPort D auxiliary channel/optional DDC. DC blocking caps must be placed on the system board.
DP_D_HPD	I	CMOS	N/A	DisplayPort D hot plug detect. 100 KΩ pull-down required on module. Protection circuitry must be placed on the system board.

3.3.4 LVDS Signal Group

The LVDS signal group provides the interface for connecting one legacy digital display (LVDS, DVI, HDMI or DisplayPort). Support for 18-bit/24-bit dual-link LVDS, HDMI, dual-link DVI and DisplayPort support is optional.

Table 3.8: Pin Description (LVDS Group)

Signal Name	I/O	Type	Impedance	Description
LVDS_LTXx LVDS_LTXx#	O	Diff	90 Ω diff	LVDS/DVI/HDMI output for single and dual-link displays (lower/odd link) Dual-mode DisplayPort E. DC blocking caps must be placed on the system board.
LVDS_LTX3 LVDS_LTX3#	I/O	Diff / OD	90 Ω diff	LVDS output for single and dual-link 24-bit displays (lower/odd link) DisplayPort E auxiliary channel/DDC. DC blocking caps must be placed on the system board. Refer to Section 3.4.5 for Dual-mode support.
LVDS_LCLK LVDS_LCLK#	O	Diff	90 Ω diff	LVDS/DVI/HDMI clock output for single and dual-link displays (lower/odd link) Dual-mode DisplayPort E. DC blocking caps must be placed on the system board.
LVDS_UTXx LVDS_UTXx#	O	Diff	90 Ω diff	LVDS/DVI/HDMI output for single and dual-link displays (upper/even link) Dual-mode DisplayPort F. DC blocking caps must be placed on the system board.
LVDS_UTX3 LVDS_UTX3#	I/O	Diff / OD	90 Ω diff	LVDS output for single and dual-link 24-bit displays (upper/even link) DisplayPort F auxiliary channel/DDC. DC blocking caps must be placed on the system board. Refer to Section 3.4.5 for Dual-mode support.
LVDS_UCLK LVDS_UCLK#	O	Diff	90 Ω diff	LVDS/DVI/HDMI clock output for single and dual-link displays (upper/even link) Dual-mode DisplayPort F. DC blocking caps must be placed on the system board.
LVDS_L_HPD	I	CMOS	N/A	DisplayPort E Hot plug detect. 100 KΩ pull-down required on module. Protection circuitry must be placed on the system board.
LVDS_U_HPD	I	CMOS	N/A	DisplayPort F Hot plug detect. 100 KΩ pull-down required on module. Protection circuitry must be placed on the system board.

Table 3.9: Pin Description (LVDS Group, continued)

Signal Name	I/O	Type	Impedance	Description
LVDS_DDC_CLK LVDS_DDC_DAT	I/O	OD	N/A	DDC clock/data for the LVDS/DVI/HDMI port. 4.7 KΩ pull-up to 3.3 V required on module. Serial devices embedded in the system board, if present, must be on this bus. System board must provide a parallel equivalent of 4.3 KΩ (± 10%). Refer to the *MXM Version 3.0 System Design Guide* for details.

Note: The LVDS_DDC bus may also be used to connect serial devices embedded in the system board. In this case, to ensure system integrity, the bus must not be connected to any external (user accessible) connector.

3.3.5 Analog Display Signal Group

The analog display signal group provides the interface for connecting one legacy analog display (CRT/TV). Support for standard CRT is required. Composite, S-Video and Component TV-Out support is optional.

Table 3.10: Pin Description (Analog Display Group)

Signal Name	I/O	Type	Impedance	Description
VGA_RED	O	Analog	50 Ω SE	Analog VGA red channel. Multiplexed with S-video chroma (C) or HDTV Pr if TV is supported.
VGA_GREEN	O	Analog	50 Ω SE	Analog VGA green channel. Multiplexed with S-video luma (Y) or HDTV Y if TV is supported.
VGA_BLUE	O	Analog	50 Ω SE	Analog VGA blue channel. Multiplexed with composite (CVBS) or HDTV Pb if TV is supported.
VGA_VSYNC	O	CMOS	50 Ω SE	Analog VGA vertical sync signal. Level shifters on the system board should be used if 5 V signaling is desired.
VGA_HSYNC	O	CMOS	50 Ω SE	Analog VGA horizontal sync signal. Level shifters on the system board should be used if 5 V signaling is desired.
VGA_DDC_CLK VGA_DDC_DAT	I/O	OD	N/A	DDC clock/data for the VGA port. 4.7 KΩ pull-up to 3.3 V required on module. System board must provide a parallel equivalent of 4.3 KΩ. Refer to the *MXM Version 3.0 System Design Guide* for details.

3.3.6 Power and Thermal Management Signal Group

Table 3.11: Pin Description (Power and Thermal Management Group)

Signal Name	I/O	Type	Impedance	Description
SMB_CLK SMB_DAT	I/O	OD	N/A	SMBus clock/data. Pull-up resistor to 3.3 V of appropriate value is required on the system board. Weak 100 KΩ pull-up to 3.3 V recommended on module. Refer to Section 3.4.12 for details.
TH_OVERT#	O	OD	N/A	Thermal shutdown request. System must power down the MXM module within 500 ms to prevent permanent damage. Pull-up resistor to 3.3 V of appropriate value is required on the system board. Weak 100 KΩ pull-up to 3.3 V recommended on module. Refer to Section 3.4.13 for details.
TH_ALERT#	I/O	OD	N/A	Thermal interrupt request. Signal may be used by the system to signal to module to reduce power consumption. The signal may also be used by the module to signal to the system a non critical temperature alert. Pull-up resistor to 3.3 V of appropriate value is required on the system board. Weak 100 KΩ pull-up to 3.3 V required on module. Refer to Section 3.4.13 for details.
TH_PWM	O	CMOS	N/A	Thermal PWM. This signal may be used to control a fan connected to the module thermal solution. Refer to Section 3.4.13 for details.
PWR_LEVEL	I	OD	N/A	Signals the module to switch to a lower power state. Modules must reduce power within 50 ms. Weak 100 KΩ pull-up to 3.3 V required on module. Power levels may be configured using software. Refer to Section 3.4.14 for details.
PWR_EN	I	CMOS	N/A	Module power enable. System must assert this signal to power on the module. May be asserted only after all input rails are within the specified tolerance. Refer to Section 3.4.1 for timing details.
PWR_GOOD	O	OD	N/A	Power sequencing sideband. The module will assert this signal when all its internal power regulators are within the required tolerance. 10 KΩ pull-up required on the system board if the feature is used.

3.3.7 System Management Signal Group

Sideband signals to control an internal panel are also included in this group. The sideband signals may be used in conjunction with any digital display interface (including DisplayPort from the DP group).

Table 3.12: Pin Description (System Management Group)

Signal Name	I/O	Type	Impedance	Description
PNL_PWR_EN	O	CMOS	N/A	Internal panel power enable. Refer to Section 3.4.15 for detailed timing requirements.
PNL_BL_EN	O	CMOS	N/A	Internal panel backlight enable.
PNL_BL_PWM	O	CMOS	N/A	Internal panel PWM brightness control.
GPIOx	I/O	CMOS	N/A	Generic GPIO pins. May be configured using the MXM software. Refer to the *MXM Graphics Module Software Specification* for details.
HDMI_CEC	I/O	OD	N/A	HDMI 1-wire CEC bus. Pull-up resistor to 3.3 V of appropriate value is required on the system board (if supported). Weak 100 KΩ pull-up to 3.3 V recommended on module.
VGA_DISABLE#	I	OD	N/A	GPU PCI class code select pin. Weak pull-up resistor required on module if the feature is implemented. Used for multi-GPU configurations. Available values are VGA (default) for a primary display adapter or non-VGA device (tied to GND on the system board) for a secondary adapter. Refer to Section 3.4.16 for details.
27MHZ_REF	I	CMOS	50 Ω SE	System 27 MHz reference clock. Refer to Section 3.4.17 for details.
WAKE#	I/O	OD	N/A	System wake and Optimized Buffer Flush/Fill (OBFF) signal. The module may assert this signal to force the system to resume from suspend (ACPI G1-S1, S2, S3, S4) or from soft-off (ACPI G2-S5). The system may signal to the module PCI-Express functions in conjunction with OBFF mechanism. If Wake and/or OBFF is supported a pull-up resistor is required on the system board. Refer to Section 3.4.18 for details.
PRSNT_R# PRSNT_L#	O	OD	N/A	MXM module present detect. Weak pull-up required on system if module detection is desired. Module must connect to ground.

Table 3.13: Pin Description (System Management Group, continued)

Signal Name	I/O	Type	Impedance	Description
JTAG_TDI	I	CMOS	N/A	Test Data In is used to serially shift test data and instructions into the device during Test Access Port (TAP) operation
JTAG_TDO	O	CMOS	N/A	Test Data Out is used to serially shift test data and instructions of the device during TAP operation
JTAG_TCLK	I	CMOS	N/A	Test Clock is used to clock test data and state information into and out of the device during TAP operation
JTAG_TMS	I	CMOS	N/A	Test Mode Select is used to control the state of the device's TAP controller
JTAG_TESTEN	I	CMOS	N/A	Test Enable is used to enable TAP operation
JTAG_TRST#	I	CMOS	N/A	Test Reset provides an asynchronous initialization of the device's TAP controller
OEMx (8 pins)	I/O	N/A	N/A	OEM reserved pins. System may connect these pins to extend the MXM functionality or to obtain cost reductions. Compliant MXM modules must not connect to any of the OEM pins. Refer to Section 3.4.19 for details.
RSVD (14 pins)	I/O	N/A	N/A	Reserved pins for future use. System must not connect any of these pins to ensure compatibility with future MXM versions. MXM version 3.1 modules must not connect to these pins.

3.4 System Requirements

This section describes the system requirements necessary to support MXM version 3.1 modules.

Note: In all timing diagrams signals should be considered unstable/unknown in gray shaded areas.

3.4.1 Power Sequencing

There is no power sequencing requirement for the input voltages to the MXM module. However the PWR_EN signal may be asserted only after all power rails are within specified tolerance. The state of PWR_GOOD is undefined until all rails are fully ramped. Refer to Figure 3.4 for details.

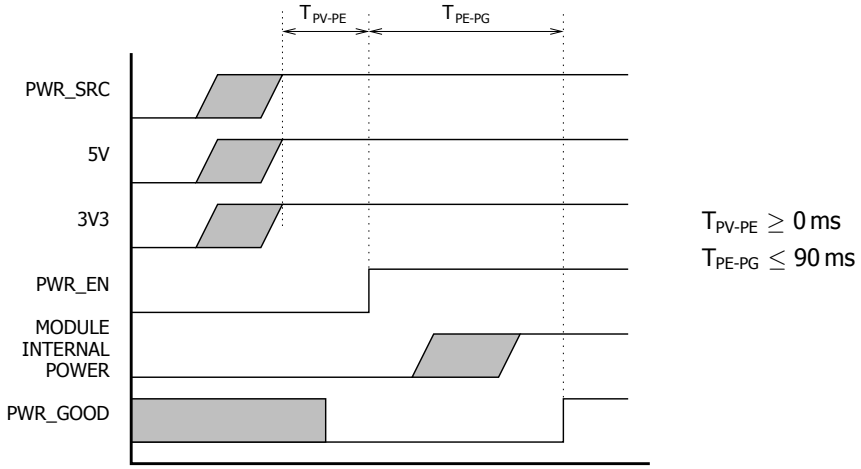


Figure 3.4: Power Sequencing

Note: No voltage shall be applied to any MXM module signal pin (except power pins and open drain signals specified in Table 3.14) until PWR_GOOD is asserted.

Table 3.14: Signals Exempted from Gating Requirement

Group	Signals
Power and Thermal	SMB_CLK, SMB_DAT TH_OVER#, TH_ALERT# PWR_GOOD
System Management	WAKE#, PEX_CLK_REQ#
Display	DP_x_HPD, LVDS_x_HPD

3.4.2 Module Power Down and Power Up

The MXM module may be powered down using the PWR_EN signal. The system designer may choose to shut down or keep the input power while the module is powered down. Refer to Figure 3.5 for details.

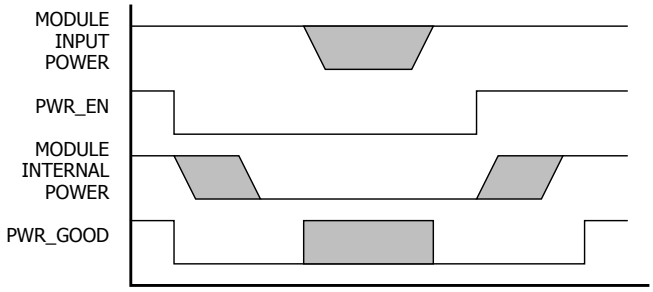


Figure 3.5: Module Power Down

Note: All output signals from the MXM module are undefined when PWR_GOOD is deasserted or undefined. The system is recommended to gate critical signals using an appropriate qualifier.

3.4.3 Reset Requirements

System reset may be deasserted only after the assertion of the PWR_GOOD signal. Figure 3.6 shows the reset requirements relative to the PWR_EN and PWR_GOOD signals. This sequence must be followed on initial power on, system reset and resume from suspend/hibernate.

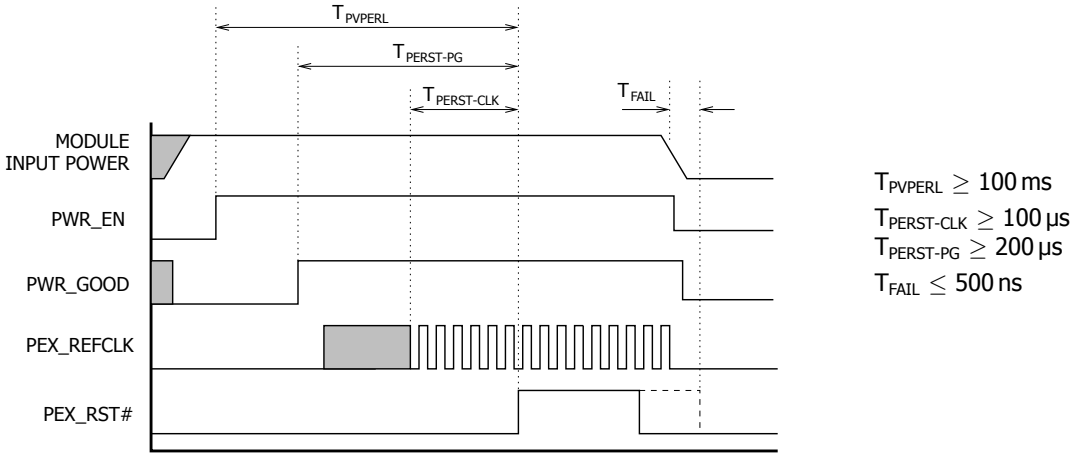


Figure 3.6: Reset Sequencing

Note: In order to reduce boot time, a system that monitors the PWR_GOOD signal, is allowed to violate the T_{PVPERL} specification as long as the $T_{PERST-PG}$ timing is still met.

3.4.4 PCI Express Interface

PCIe traces must be routed with the impedance specified by Table 3.6. DC blocking capacitors for both TX and RX lines must be placed on the system board. Refer to the *PCI Express Base Specification* for specific capacitors requirements.

Note: Note: Capacitance value requirements are different for 8 GT/s.

3.4.5 DisplayPort Interface

DisplayPort traces must be routed with the impedance specified by Table 3.7. DC blocking capacitors must be placed on the system board. In addition the MXM implementation of Dual-mode DisplayPort requires the circuit in Figure 3.7 on the AUX lines for proper dongle detection. The HPD signal conditioning must also be placed on the system board.

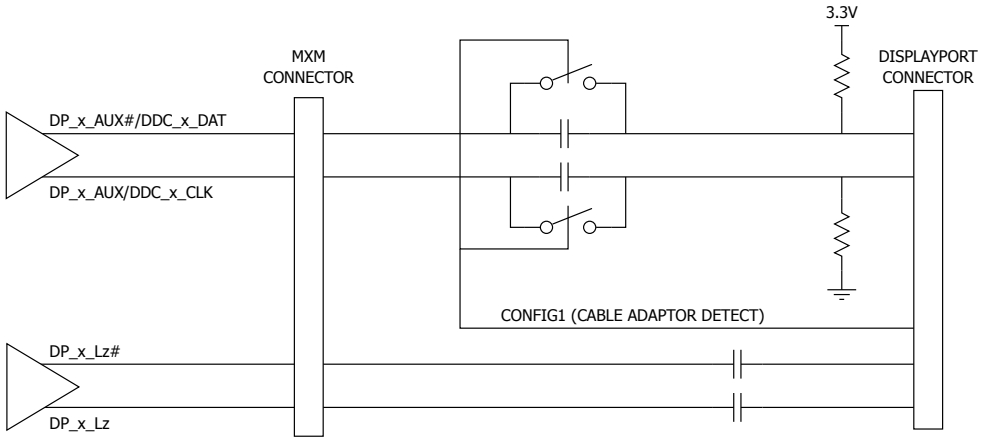


Figure 3.7: Dual-mode DisplayPort Implementation

3.4.6 Embedded Display Port (eDP)

Support for embedded DisplayPort (eDP) is an optional feature, however if the module supports eDP, the feature is recommended to be available on all implemented DisplayPorts. Dual Mode DP functionality (support for DVI/HDMI dongles), if available, must be disabled by the module software for any port configured as eDP by the MXM SIS.

3.4.7 DVI/HDMI on DP Interface

Native DVI or HDMI connector support can be implemented using a display port interface. Additional circuitry is required on the system and the proper signal mapping must be observed. As Figure 3.8 shows, 499 Ω 1% pull-down resistors to ground on the DP lane signals must be placed on the connector side of the AC coupling capacitors gated by a FET to limit the leakage. Additionally level shifting circuits must also be implemented on DDC Data and Clock, refer to the *MXM Version 3.0 System Design Guide* for specific details.

Table 3.15 shows the mapping to connect the signals from the MXM connector to the HDMI/DVI connector. For the optional dual-link DVI support refer to Table 3.16.

Table 3.15: DisplayPort Multiplexed Signal Definition

Pin Name	DVI/HDMI
DP_x_L0 DP_x_L0#	TX_x_D2 TX_x_D2#
DP_x_L1 DP_x_L1#	TX_x_D1 TX_x_D1#
DP_x_L2 DP_x_L2#	TX_x_D0 TX_x_D0#
DP_x_L3 DP_x_L3#	TX_x_CLK TX_x_CLK#
DP_x_AUX	DDC_x_CLK
DP_x_AUX#	DDC_x_DAT

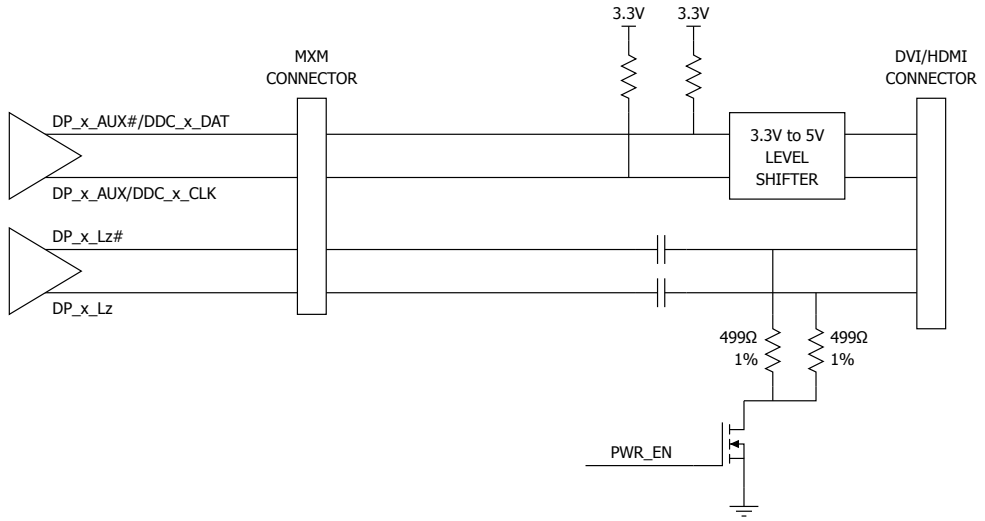


Figure 3.8: DVI/HDMI Implementation using DP Interface

Table 3.16: Dual-Link DVI

Dual-Link DVI	DP_A+DP_B	DP_A+DP_C	DP_C+DP_D	DP_E+DP_F
TX_CLK	DP_A_L3	DP_A_L3	DP_C_L3	DP_E_L3
TX_D0	DP_A_L2	DP_A_L2	DP_C_L2	DP_E_L2
TX_D1	DP_A_L1	DP_A_L1	DP_C_L1	DP_E_L1
TX_D2	DP_A_L0	DP_A_L0	DP_C_L0	DP_E_L0
TX_D3	DP_B_L2	DP_C_L2	DP_D_L2	DP_F_L2
TX_D4	DP_B_L1	DP_C_L1	DP_D_L1	DP_F_L1
TX_D5	DP_B_L0	DP_C_L0	DP_D_L0	DP_F_L0
DDC	DP_A_AUX	DP_A_AUX	DP_C_AUX	DP_E_AUX

3.4.8 DVI/HDMI/DP on LVDS Interface

The MXM module can optionally provide DVI/HDMI/DP output through the LVDS signal port. The signal mapping for this multifunctional port is defined in Table 3.17.

Table 3.17: LVDS Multiplexed Signal Definition

Pin Name	HDMI	Dual-link DVI	DP
LVDS_LTX0 LVDS_LTX0#	TX_D0 TX_D0#	TX_D0 TX_D0#	DP_E_L2 DP_E_L2#
LVDS_LTX1 LVDS_LTX1#	TX_D1 TX_D1#	TX_D1 TX_D1#	DP_E_L1 DP_E_L1#
LVDS_LTX2 LVDS_LTX2#	TX_D2 TX_D2#	TX_D2 TX_D2#	DP_E_L0 DP_E_L0#
LVDS_LTX3 LVDS_LTX3#	N/A	N/A	DP_E_AUX DP_E_AUX#
LVDS_LCLK LVDS_LCLK#	TX_CLK TX_CLK#	TX_CLK TX_CLK#	DP_E_L3 DP_E_L3#
LVDS_L_HPD	HDMI_HPD	DVI_HPD	DP_E_HPD
LVDS_UTX0 LVDS_UTX0#	N/A	TX_D3 TX_D3#	DP_F_L2 DP_F_L2#
LVDS_UTX1 LVDS_UTX1#	N/A	TX_D4 TX_D4#	DP_F_L1 DP_F_L1#
LVDS_UTX2 LVDS_UTX2#	N/A	TX_D5 TX_D5#	DP_F_L0 DP_F_L0#
LVDS_UTX3 LVDS_UTX3#	N/A	N/A	DP_F_AUX DP_F_AUX#
LVDS_UCLK LVDS_UCLK#	N/A	N/A	DP_F_L3 DP_F_L3#
LVDS_U_HPD	N/A	N/A	DP_F_HPD
LVDS_DDC_CLK LVDS_DDC_DAT	DDC_CLK DDC_DAT	DDC_CLK DDC_DAT	N/A

3.4.9 VGA Interface

The system motherboard should route all VGA signals (R, G, B, and Sync) with 50 Ω impedance. A 150 Ω termination resistor to ground should be placed at the end of the RGB traces as close as possible to the output filters as depicted in Figure 3.9.

The MXM module must route all VGA signals with 50 Ω impedance as well and place a 150 Ω termination resistor to ground as close as possible to the RGB signal drivers as shown in Figure 3.9.

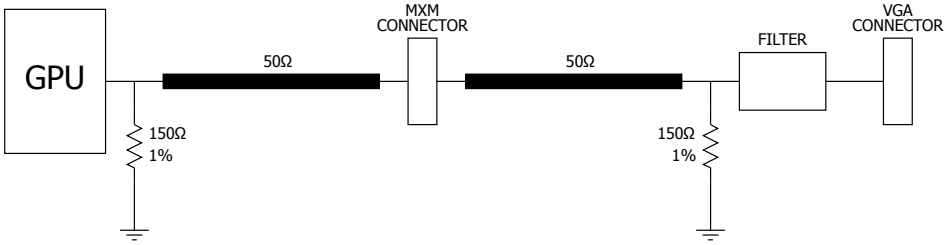


Figure 3.9: VGA Implementation

3.4.10 TV Out

The VGA and TV signals share the same pins at the MXM connector. Therefore, a demultiplexer is needed on the motherboard if the system supports both VGA and TV out. Refer to Figure 3.10 for a simplified schematics.

The motherboard should route all signals with 50 Ω impedance. A 150 Ω termination resistor to ground should be placed at the end of the trace before the demultiplexer as shown in Figure 3.10.

For the MXM module there are no additional requirements to support TV Out as long as the VGA interface is correctly implemented (refer to Section 3.4.9).

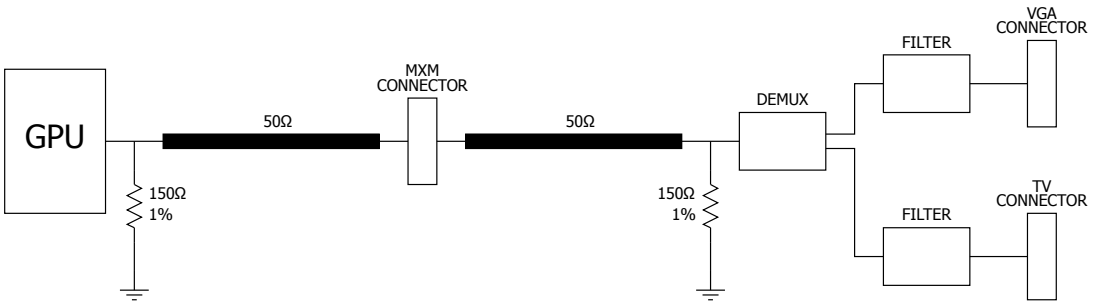


Figure 3.10: TV Implementation

3.4.11 DVI-I Support

MXM supports combining any TMDS capable digital link with the VGA interface to provide DVI-I functionality. Table 3.18 shows all the allowed configurations with the associated DDC channel mapping.

Table 3.18: DVI-I DDC Mapping

Configuration	Digital Link	DDC	Notes
Single link	DP_A	DP_A_AUX	Required
Single link	DP_B	DP_B_AUX	Optional
Single link	DP_C	DP_C_AUX	Required
Single link	DP_D	DP_D_AUX	Optional
Single link	DP_E	DP_E_AUX	Required
Single link	DP_F	DP_F_AUX	Optional
Single link	LVDS_L	LVDS_DDC	Optional
Dual link	LVDS_L+LVDS_U	LVDS_DDC	Optional
Dual link	DP_A+DP_B	DP_A_AUX	Optional
Dual link	DP_C+DP_D	DP_C_AUX	Optional
Dual link	DP_A+DP_C	DP_A_AUX	Optional
Dual link	DP_E+DP_F	DP_E_AUX	Optional

3.4.12 SMBus interface

The MXM version 3.1 module shall connect a thermal sensor, compatible to the MAX6649 or LM99, to the SMBus for reading the GPU die temperature. The system must be able to access the GPU die temperature at any of the four possible SMBus addresses 0x98, 0x9E, 0x56, or 0x32. The module must respond to at least one of the addresses but may at the designer option respond to multiple or all of them. The MXM module may include MXM MIS at any of the module SMBus address. The SMBus address shown here is the 8-bit address, where the seven most significant bits are the address and the least significant bit is the read/write bit.

Table 3.19: Module SMBus Address

SMBus Address	7-bit Address	Write Address	Read Address
0x98	1001100	0x98	0x99
0x9E	1001111	0x9E	0x9F
0xA0	1010000	0xA0	0xA1
0x56	0101011	0x56	0x57
0x32	0011001	0x32	0x33

Note: No SMBus system devices are allowed to respond to the MXM reserved addresses. Separate SMBus buses or isolation circuitry is required to avoid conflicts.

3.4.13 Thermal and Power Management Interface

The thermal and power management interface of the MXM module consists of three main control signals in addition to the SMBus interface used to read temperature and control various inputs to the temperature and power management interface.

The three control signals can be described as system thermal and power protection (TH_OVERT#) and thermal and power system optimization (TH_ALERT# and TH_PWM).

TH_OVERT# is a required open drain output from the MXM module which alerts the system that a critical temperature threshold has been crossed and the system must be shut down within 500 ms to prevent physical damage. The temperature threshold is defined as the minimum value of the module and the system limits (refer to the *MXM Graphics Module Software Specification* for details). This feature is a fail-safe and should not occur during normal operation.

TH_ALERT# is an optional open drain input/output of the MXM module. On the MXM module side, the module will assert this signal to notify the system that its ALERT temperature has been crossed and it is taking steps to reduce the temperature and power of the module. On the system side, if the system determines the MXM module is operating in a temperature and power range it should not be, the system can assert the TH_ALERT# input to invoke the same temperature reduction mechanism to lower the temperature and power of the module.

TH_PWM is an optional output of the MXM module which can be used to control a fan to optimize the MXM module performance and acoustic characteristics. The PWM frequency must be programmable between 10 and 30,000 Hz with duty cycle steps of no more than 1%. Refer to the *MXM Graphics Module Software Specification* for details.

3.4.14 PWR_LEVEL Signal

The purpose of this pin is to give the system a hardware method for signaling the module to reduce power consumption. The logic states are defined as 1 for full power and 0 for reduced power. These two states may correspond to two power levels defined in the MXM System Information Structure (input power substructure). Refer to the *MXM Graphics Module Software Specification* for more information on this substructure. Alternatively the module implementer may choose to associate the pin states with other methods of power reduction. In any case the support of this feature is required for the module and must provide at least 20% power reduction from full power to reduced power. The use of this feature is optional for the system (may be left unconnected).

When PWR_LEVEL transitions from 1 to 0, the module must reduce power consumption within 50 ms. In transitions from 0 to 1 the module may return to the full power state within 250 ms.

The system should determine the values of the two power levels in the structure based on the considerations of the maximum allowable current (10 A) through the PWR_SRC rail limited by the capability of the MXM connector, and the maximum allowable current of the battery. The system should drive PWR_LEVEL low whenever a condition occurs that may cause the current through PWR_SRC to exceed 10 A, or the total current drawn from the battery to exceed its limit. An example would be that the AC adapter is inadvertently unplugged and the battery is running at a lower voltage. In this case, the module, maintaining its higher power level, may draw a current greater than 10 A and damage the connector. Another example is a system that contains more than one MXM module and operates at full power of each module. When the AC adapter is unplugged in this case, the individual module may not draw current more than 10 A but the total current drawn from the battery may exceed its limit. If the modules do not transition from high to low power in time, the battery may be damaged.

3.4.15 Internal Flat Panel Interface

The flat panel sideband signals may be used for any type of internal panel (LVDS/TMDS/eDP). For LVDS and TMDS displays the MXM module must meet the timing specification detailed in Figure 3.11. For eDP displays the module must meet the eDP interface power Up/Down sequence defined in the *VESA Embedded Display Port (eDP)* specification.

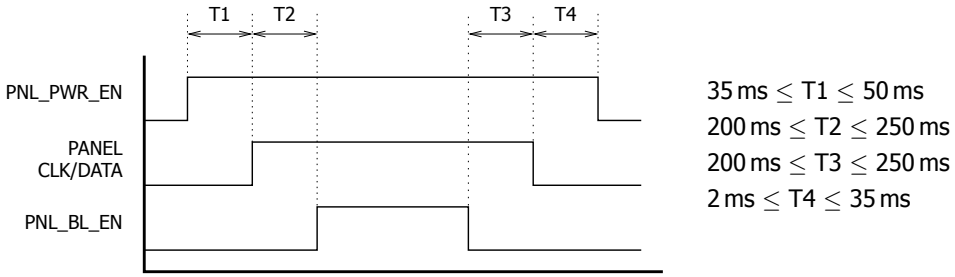


Figure 3.11: Internal Flat Panel Timing

3.4.16 VGA_DISABLE# Signal

This signal may be used in a system containing more than one graphics controller. The support of this feature is optional for both the system and the module.

Systems with multiple graphics controllers may require a hardware mechanism to determine which adapter is the boot display device. This pin, when tied to GND, will disable the VGA functionality of the MXM module to prevent it from being used as a boot display device. The MXM module, depending on the logic state of this signal, will configure its own PCI class code according to Table 3.20.

Table 3.20: VGA_DISABLE# Functionality

VGA_DISABLE# Pin	Base Class	Sub-Class	Class Code Description
NC	0x03	0x00	VGA-compatible controller
GND	0x03	0x02 or 0x80	3D controller or other display controller

3.4.17 Reference Clock

The system may provide a 27 MHz reference clock on 27MHZ_REF pin for system-module synchronization by common clock architecture. A system implementing reference clock must meet the specifications in Table 3.21 and have a corresponding structure in MXM SIS. As an example, this feature can be used for audio and video synchronization, where the audio device does not reside on the module.

Table 3.21: 27 MHz Reference Clock Specifications

Symbol	Parameter	Min	Nom	Max	Units
f_{IN}	Frequency		27		MHz
t_{DC}	Duty Cycle	45		55	%
T_{AVE}	Average Period Accuracy	-50		50	ppm
t_{CCJ}	Cycle to Cycle Jitter			150	ps

3.4.18 WAKE Functionality

The WAKE# pin is an open drain output which has been provided as a mechanism for the MXM module to wake the system from a suspend or soft-off state. To initiate and complete a WAKE event, the module must assert WAKE# and then wait for PEX_RST# to deassert which will signal the end of the electrical portion of the WAKE event. WAKE# must only be asserted by the MXM module when all of its functions are in D3 state and at least one of its functions is enabled for wakeup generation using the PME enable bit in the PMCSR. If a system supports wakeup, the 3V3 supply must be present for all device states that support wakeup. As an example, this feature can be used in conjunction with the HDMI CEC feature to wake the system on CEC events received by the MXM module while the system is in one of the suspend states or soft-off states. Another example use of this feature would be to have one of the HPD (hot plug detect) events wake the system from a suspend or soft off state when a display is connected to the MXM module. Note that the voltage the system uses to terminate WAKE# may be lower than the 3V3 voltage to be compatible with lower voltage processes of the system PM controller.

The WAKE# pin may be used by the system to signal to PCI function(s) on the module in conjunction with OBFF mechanism.

Refer to *PCI Express Card Electromechanical Specification revision 3.0* for WAKE and OBFF AC timing requirements.

3.4.19 OEM Modules

In the MXM version 3.1 connector interface, eight pins have been allocated for OEM customization of system features. An MXM version 3.1 compliant system can use these pins for any functions it defines. It achieves these functions by using an OEM customized module. This OEM module is not MXM version 3.1 compliant and can not be used in any other systems and be guaranteed to function correctly. On the other hand, any MXM version 3.1 compliant module will work correctly in any MXM version 3.1 compliant system even if the system uses OEM pins. This is achieved by requiring any MXM version 3.1 compliant module not to connect to any of the OEM pins.

3.4.20 MXM System Information Structure

Compliant systems must implement the MXM System Information Structure (SIS) as described in the *MXM Graphics Module Software Specification*. The system designer may choose to store the SIS data in either the System BIOS or in a separate I2C compatible serial ROM. If a serial ROM is used it must be connected to the LVDS_DDC bus and respond to address 0xA8. Refer to the *MXM Graphics Module Software Specification* and to the *MXM Version 3.0 System Design Guide* for details.

Note: When LVDS_DDC is used with an external monitor, the serial ROM is not recommended. The serial ROM may not fuction correctly due to some external monitors that incorrectly respond to address 0xA8.

3.4.21 MXM Module Information Structure

The module may implement the MXM Module Information Structure (MIS). Module Information data structure, which resides on the module, consists of registers and/or structures of information the system may retrieve or monitor through the SMBus (refer to Section 3.4.12). As an example, this feature can be used to monitor the stability of the memory interface by monitoring memory

errors. Another example is to monitor the temperature of power supply or memory zones and use this as input into the systems thermal control. Refer to the module manufacture for detailed register and/or structure definitions.

3.5 Signal Integrity

The MXM specification, to ensure module interoperability, defines requirements for both the module and the system interconnect.

For graphics modules, the MXM signal integrity specification follows the published specifications of each interface, except where explicitly defined. Eye diagram requirements are redefined to account for the different configuration. Other parameters are redefined due to budget allocations between modules and system boards.

For system boards, the MXM signal integrity specification is based on the total interconnect performance including the MXM connector, PCB traces, and any other connector. Insertion and return loss budgets in the form of S-parameter masks are provided for each interface. The use of S-parameters masks allows the designer to determine the best trade-offs based on the system requirements.

MXM specific test boards are required for both module and system validation. Section 3.5.1 describes the requirements for the module and Section 3.5.2 describes the requirements for the system. Subsequent sections describe the details for each interface.

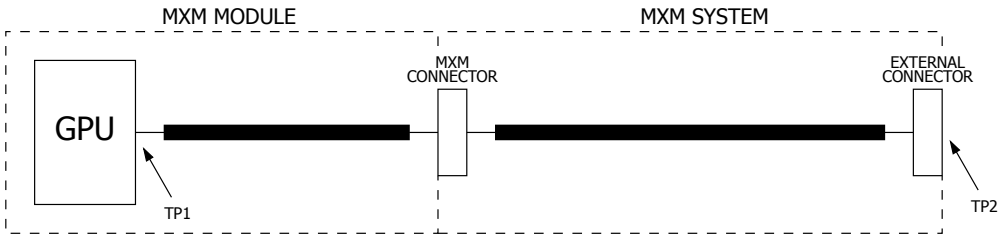


Figure 3.12: MXM Module and System

3.5.1 Module Specification

The compliance measurements for all interfaces, except DP HBR2 and PCIe 8 GT/s, must be taken at test point TP_MXM. TP_MXM is defined as the SMP connector on the Compliance Base Board (CBB). Refer to Figure 3.13 for a simplified diagram of the validation setup and Table 3.22 for the CBB specifications. The compliance measurement of DisplayPort High Bit Rate 2 must be taken at TP3EQ using a mathematical system and cable (HBR C1) model with HBR2 reference equalizer incorporated into the analyzer as shown in Figure 3.14. HBR C1 is the cable model with connector option 1 as defined in *VESA DisplayPort Standard*, Version 1, Revision 2. The compliance measurement of PCIe 8 GT/s must be taken at TP2P using a mathematical system model and behavioral RX with CTLE/DFE post processing scripts incorporated into the analyzer as shown in Figure 3.15.

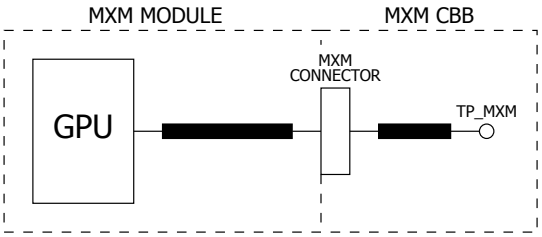


Figure 3.13: Module Validation Test Setup

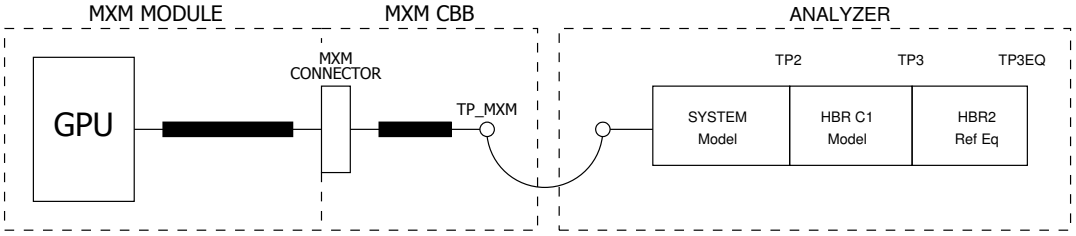


Figure 3.14: Module Validation Test Setup (DP HBR2 Interface)

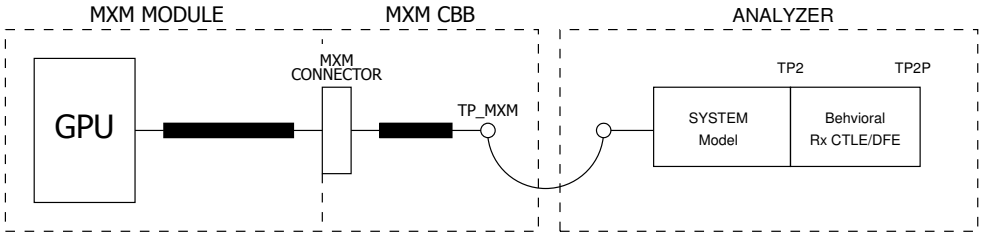


Figure 3.15: Module Validation Test Setup (PCIe 8 GT/s TX Interface)

Table 3.22: TP_MXM CBB Specification

Interface	Impedance	Trace Length	Spacing	AC CAP	Termination	Connector
DP	100 Ω diff	50 mm ± 1	4X	0.1 µF	50 Ω PD	SMP
TMDS	100 Ω diff	50 mm ± 1	4X	N/A	50 Ω PU	SMP
LVDS	100 Ω diff	50 mm ± 1	4X	N/A	100 Ω Diff	SMP
PCIe RX	85 Ω diff	75 mm ± 1	4X	N/A	NONE	SMP
PCIe TX	85 Ω diff	75 mm ± 1	4X	0.1 µF	50 Ω PD	SMP
RGB	50 Ω SE	75 mm ± 1	4X	N/A	50 Ω PD	SMP

Note: The termination requirements in Table 3.22 may be satisfied either with a resistor on the CBB PCB or, if available, with the internal termination of the measurement equipment.

3.5.2 System Specification

The compliance measurements for all interfaces, except PCIe 8 GT/s, must be taken at test point TP_SYS. TP_SYS is defined as the SMP connector on the Compliance Load Board (CLB). Two test fixtures are required to measure the signal quality of the display outputs. These test fixtures are the CLB and the External Load Board (ELB). For PCIe compliance only the CLB is required. Figure 3.16 shows the setup for the display outputs validation and Figure 3.17 shows the setup for PCIe 2.5 GT/s and 5 GT/s validation. The compliance measurement of PCIe 8 GT/s must be taken at TP2P using behavioral RX with CTLE/DFE post processing scripts incorporated into the analyzer as shown in Figure 3.18.

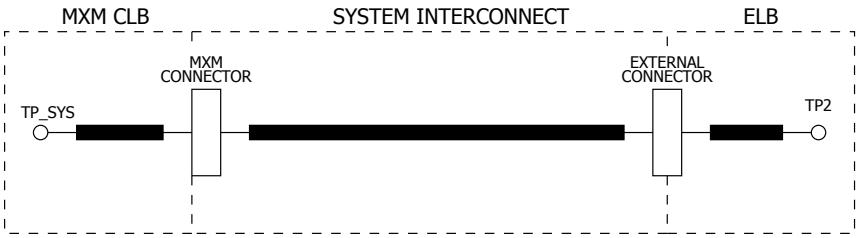


Figure 3.16: System Validation Test Setup (Display Interfaces)

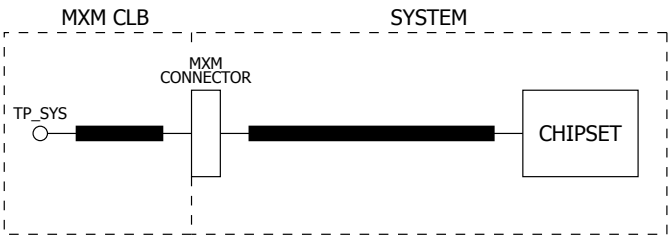


Figure 3.17: System Validation Test Setup (PCIe 2.5 GT/s and 5 GT/s Interface)

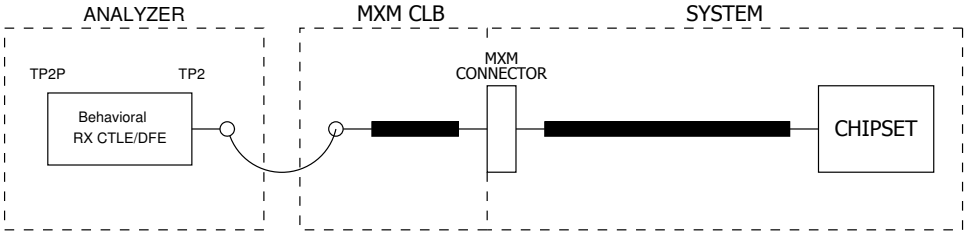


Figure 3.18: System Validation Test Setup (PCIe 8 GT/s TX Interface)

Table 3.23: MXM CLB Specification

Interface	Impedance	Trace Length	Spacing	AC CAP	Termination	Connector
DP	100 Ω diff	50 mm ± 1	4X	N/A	N/A	SMP
TMDS	100 Ω diff	50 mm ± 1	4X	N/A	N/A	SMP
LVDS	100 Ω diff	50 mm ± 1	4X	N/A	N/A	SMP
PCIe	85 Ω diff	50 mm ± 1	4X	N/A	50 Ω PD	SMP
RGB	50 Ω SE	50 mm ± 1	4X	N/A	N/A	SMP

Note: The termination requirements in Table 3.23 may be satisfied either with a resistor on the CLB PCB or, if available, with the internal termination of the measurement equipment.

Table 3.24: ELB Specification

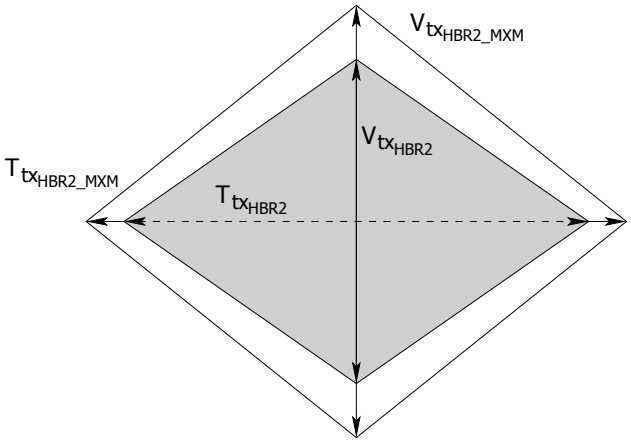
Interface	Impedance	Trace Length	Spacing	AC CAP	Termination	Connector
DP	100 Ω diff	38 mm ± 1	4X	N/A	N/A	SMP
TMDS	100 Ω diff	38 mm ± 1	4X	N/A	N/A	SMP
LVDS	100 Ω diff	38 mm ± 1	4X	N/A	N/A	SMP
RGB	50 Ω SE	38 mm ± 1	4X	N/A	N/A	SMP

3.5.3 Display Port

MXM compliant modules must meet the specification in Table 3.25 and Figure 3.20 for High Bit Rate (HBR) or Figure 3.21 for Reduced Bit Rate (RBR) at TP_MXM for all supported DisplayPorts. Modules that support High Bit Rate 2 (HBR2) must meet the eye defined in Figure 3.19 at TP3EQ.

Table 3.25: Module Specifications for DisplayPort

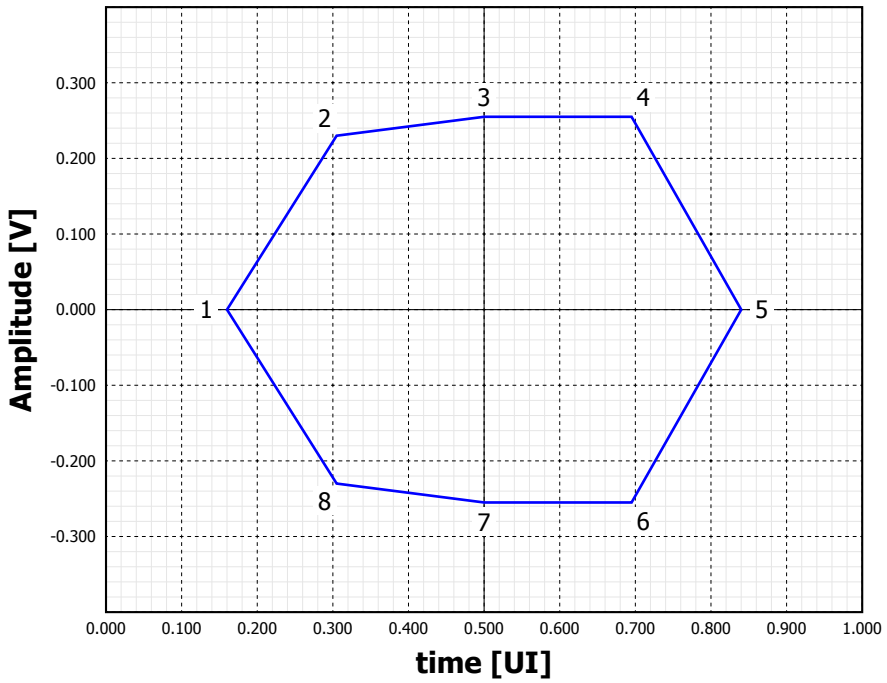
Symbol	Parameter	Min	Max	Unit	Notes
$L_{\mu ASKEW\text{-}INTER\text{-}M}$	Inter-pair skew		1.2	UI	RBR or HBR
$L_{SKEW\text{-}INTER\text{-}M}$	Inter-pair skew		2.4	UI	HBR2
$L_{SKEW\text{-}INTRA\text{-}M}$	Intra-pair skew		25	ps	informative
$V_{TX\text{-}AC\text{-}CM}$	AC common mode noise		15	mV	
$\left(\frac{V_{DIFF\text{-}PRE\text{-}v\text{-}0}}{V_{DIFF\text{-}v\text{-}0}}\right)_{dB}$	Pre-emphasis level 0		0.25	dB	v=0,1,2,3
$\left(\frac{V_{DIFF\text{-}PRE\text{-}v\text{-}1}}{V_{DIFF\text{-}v\text{-}1}}\right)_{dB} - \left(\frac{V_{DIFF\text{-}PRE\text{-}v\text{-}0}}{V_{DIFF\text{-}v\text{-}0}}\right)_{dB}$	Pre-emphasis delta 1	2.1		dB	v=0,1,2
$\left(\frac{V_{DIFF\text{-}PRE\text{-}v\text{-}2}}{V_{DIFF\text{-}v\text{-}2}}\right)_{dB} - \left(\frac{V_{DIFF\text{-}PRE\text{-}v\text{-}1}}{V_{DIFF\text{-}v\text{-}1}}\right)_{dB}$	Pre-emphasis delta 2	1.7		dB	v=0,1
$\left(\frac{V_{DIFF\text{-}PRE\text{-}0\text{-}3}}{V_{DIFF\text{-}0\text{-}3}}\right)_{dB} - \left(\frac{V_{DIFF\text{-}PRE\text{-}0\text{-}2}}{V_{DIFF\text{-}0\text{-}2}}\right)_{dB}$	Pre-emphasis delta 3	1.7		dB	



Parameter	Min	Max	Unit
$V_{tx_{HBR2\ MXM}}$	$V_{tx_{HBR2}}$ + 28		mV
$T_{tx_{HBR2\ MXM}}$	$T_{tx_{HBR2}}$ + 0.06		UI

Figure 3.19: DisplayPort HBR2 TP3EQ Eye Diagram

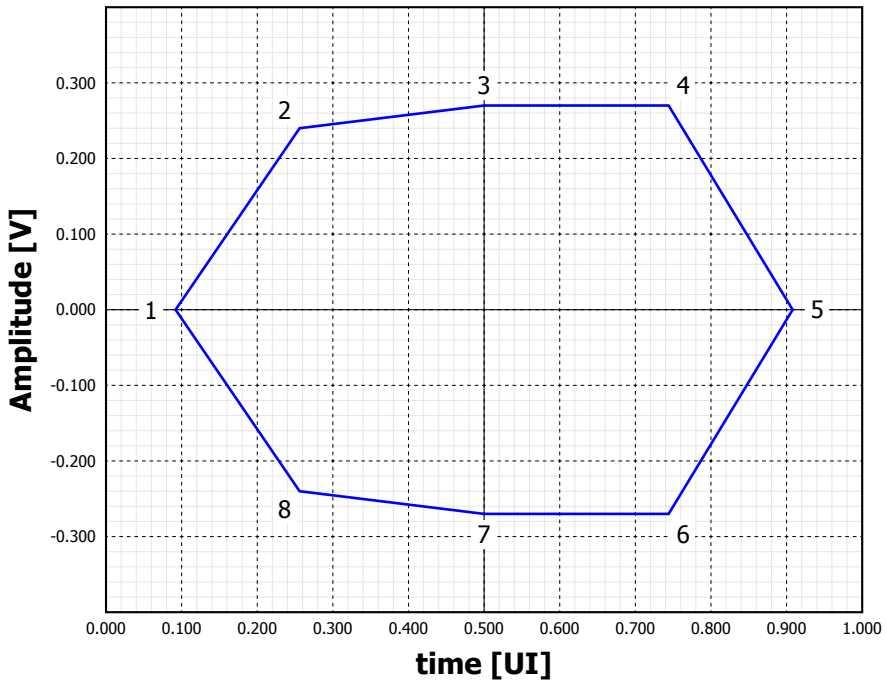
Note: $V_{tx_{HBR2}}$ and $T_{tx_{HBR2}}$ are the differential peak-to-peak eye voltage and eye width (1 - Maximum_TX_Total_Jitter), respectively. Where differential peak-to-peak eye voltage and maximum tx total jitter are defined in *VESA DisplayPort Standard*, Version 1, Revision 2, Main TX TP3 EQ table.



Point	t [UI]	A [V]
1	0.160	0.000
2	0.305	0.230
3	0.500	0.255
4	0.695	0.255
5	0.840	0.000
6	0.695	-0.255
7	0.500	-0.255
8	0.305	-0.230

Jitter [UI]	
Non-ISI	0.265
Tj	0.320

Figure 3.20: DisplayPort HBR TP_MXM Eye Diagram



Point	t [UI]	A [V]
1	0.092	0.000
2	0.256	0.240
3	0.500	0.270
4	0.744	0.270
5	0.908	0.000
6	0.744	-0.270
7	0.500	-0.270
8	0.256	-0.240

Jitter [UI]	
Non-ISI	0.165
Tj	0.200

Figure 3.21: DisplayPort RBR TP_MXM Eye Diagram

The DisplayPort and eDP interconnect on an MXM compliant system supporting up to HBR must meet the specifications in Table 3.26 and Figure 3.23. A system supporting HBR2 must meet the specifications in Table 3.26 and Figure 3.22 including an additional parameter, power sum equal level far-end noise (PSELFEN) as defined in the following equations.

$$PSFEN(f) = 10 \times log \sum_{1}^{n} 10^{\left(\frac{FENn(f)}{10}\right)}$$

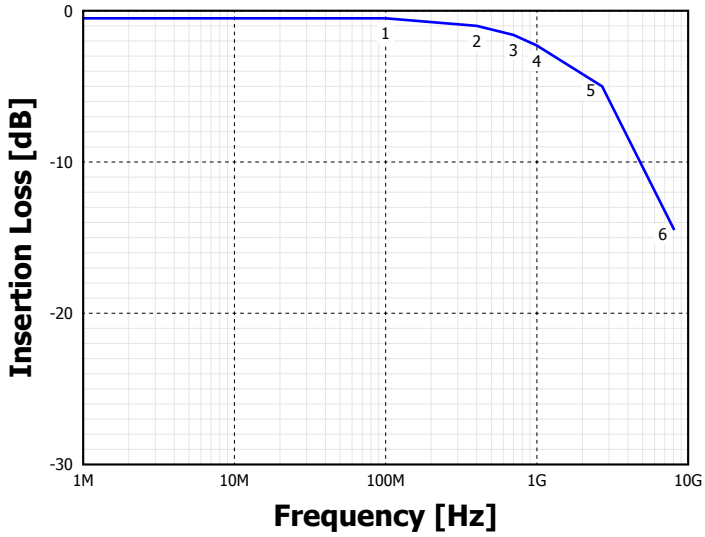
$$PSELFEN(f) = PSFEN(f) - IL(f)$$

Where:

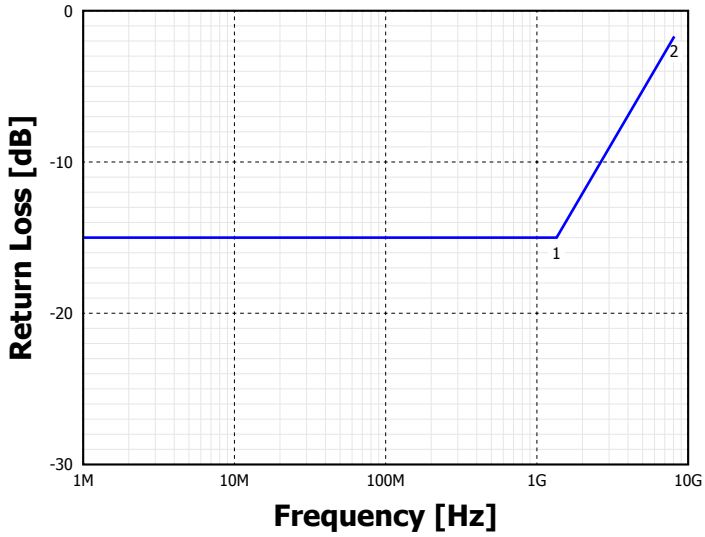
FENn(f) is the far-end noise in dB
IL(f) is the victim lane insertion loss in dB

Table 3.26: System Board Specifications for DisplayPort

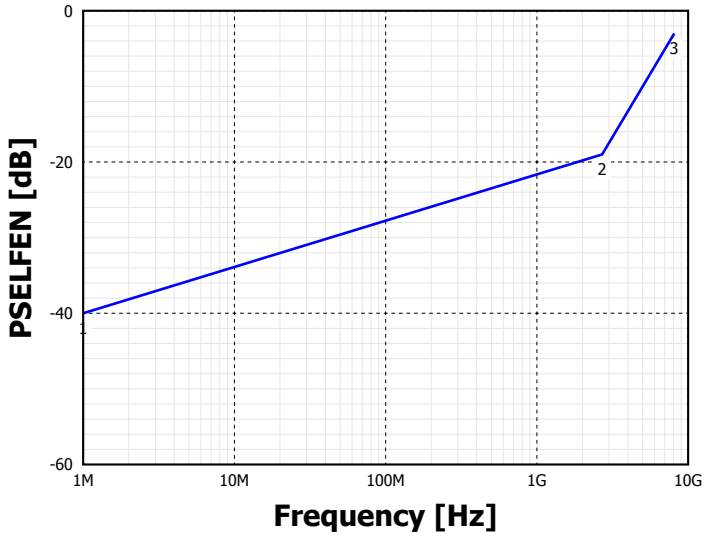
Symbol	Parameter	Min	Max	Unit	Notes
$L_{SKEW-INTER-S}$	Inter-pair skew		0.8	UI	RBR or HBR
$L_{SKEW-INTER-S}$	Inter-pair skew		1.6	UI	HBR2
$L_{SKEW-INTRA-S}$	Intra-pair skew		5	ps	



Point	f [MHz]	Loss [dB]
1	100	-0.5
2	400	-1.0
3	700	-1.6
4	1000	-2.3
5	2700	-5.0
6	8100	-14.5

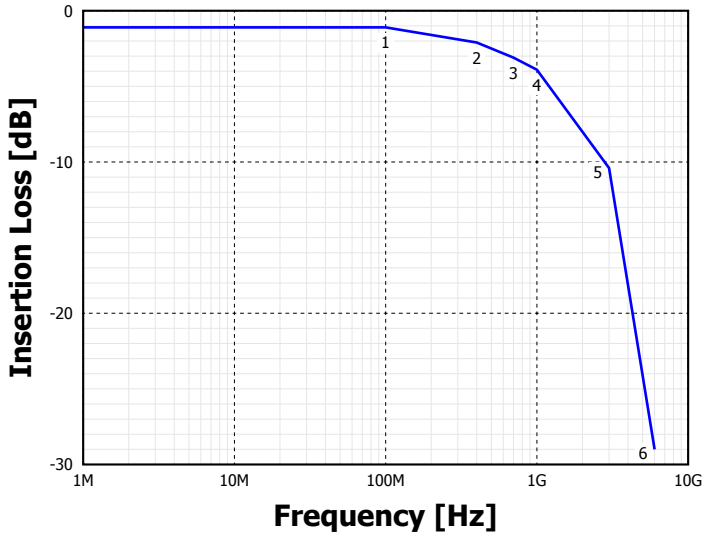


Point	f [MHz]	Loss [dB]
1	1350	-15
2	8100	-1.7

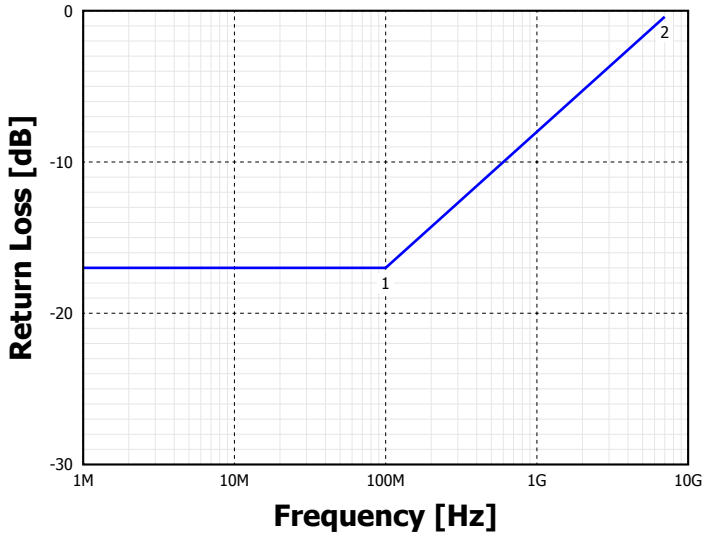


Point	f [MHz]	PSELFEN [dB]
1	1	-40
2	2700	-19
3	8100	-3

Figure 3.22: System Board Insertion Loss, Return Loss, and PSELFEN Requirements for DisplayPort HBR2



Point	f [MHz]	Loss [dB]
1	100	-1.1
2	400	-2.1
3	700	-3.1
4	1000	-3.9
5	3000	-10.4
6	6000	-29.0



Point	f [MHz]	Loss [dB]
1	100	-17
2	7000	-0.4

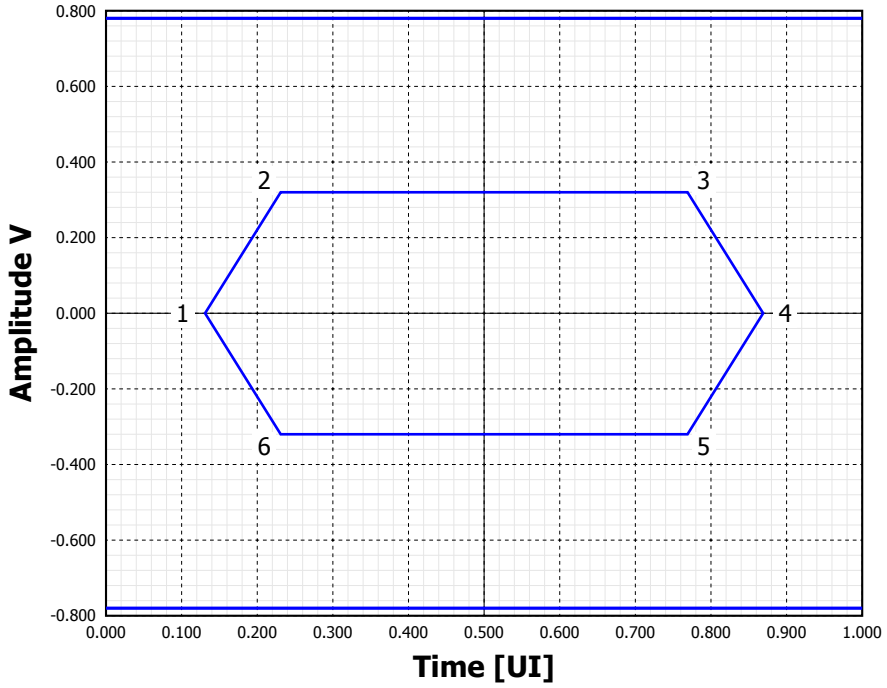
Figure 3.23: System Board Insertion and Return Loss Requirements for DisplayPort RBR and HBR

3.5.4 TMDS

All supported TMDS ports on the MXM module must meet the specification in Table 3.27, Figure 3.24 and Figure 3.25.

Table 3.27: Module Specifications for TMDS

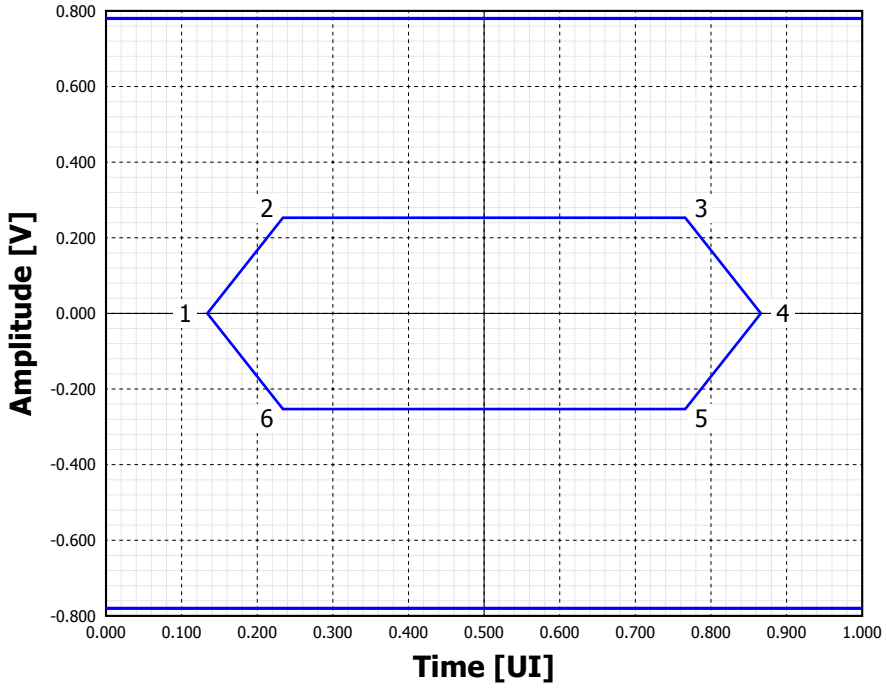
Symbol	Parameter	Min	Max	Unit	Notes
$T_{SKEW-INTER-M}$	Inter-pair skew		0.8	UI	
$T_{SKEW-INTRA-M}$	Intra-pair skew		0.1	UI	
Tj	Clock jitter		0.16	UI	
T_{DUTY}	Clock duty cycle	40	60	%	HDMI only
T_{RISE}/T_{FALL}	Rise/Fall times	75	0.35	ps/UI	
V_{DIFF}	Differential swing	860	1200	mV	
V_L	Single-ended low voltage level	A_{Vcc}-600	A_{Vcc}-400	mV	HDMI only
V_{OFF}	Single-ended standby voltage	A_{Vcc}-10	A_{Vcc}+10	mV	HDMI only
	Overshoot		15	%	
	Undershoot		20	%	
	DDC SCL/SDA capacitance		15	pF	HDMI only
	CEC line capacitance		50	pF	HDMI only



Point	t [UI]	A [V]
1	0.131	0.000
2	0.231	0.320
3	0.769	0.320
4	0.869	0.000
5	0.769	-0.320
6	0.231	-0.320

Absolute Amplitude Limits [V]	
$V_{ABS\ MAX}$	0.780
$V_{ABS\ MIN}$	-0.780

Figure 3.24: TMDS/HDMI $\leq$ 225MHz TP_MXM Eye Diagram



Point	t [UI]	A [V]
1	0.134	0.000
2	0.234	0.253
3	0.766	0.253
4	0.866	0.000
5	0.766	-0.253
6	0.234	-0.253

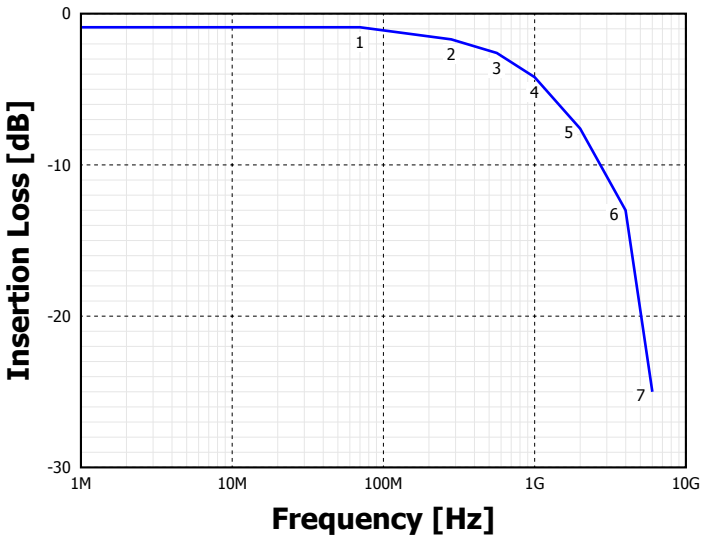
Absolute Amplitude Limits [V]	
$V_{ABS\ MAX}$	0.780
$V_{ABS\ MIN}$	-0.780

Figure 3.25: HDMI > 225MHz TP_MXM Eye Diagram

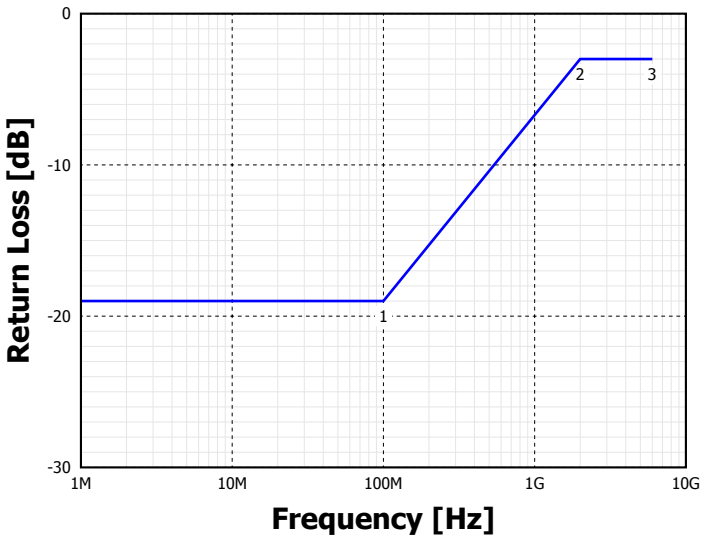
The TMDS interconnect on a MXM compliant system must meet specifications in Table 3.28, Figure 3.26 and Figure 3.27.

Table 3.28: System Board Specifications for TMDS

Symbol	Parameter	Min	Max	Unit	Notes
$T_{SKEW-INTER-S}$	Inter-pair skew		1.2	UI	
$T_{SKEW-INTRA-S}$	Intra-pair skew		0.05	UI	
	DDC SCL/SDA capacitance		35	pF	HDMI only
	CEC line capacitance		100	pF	HDMI only

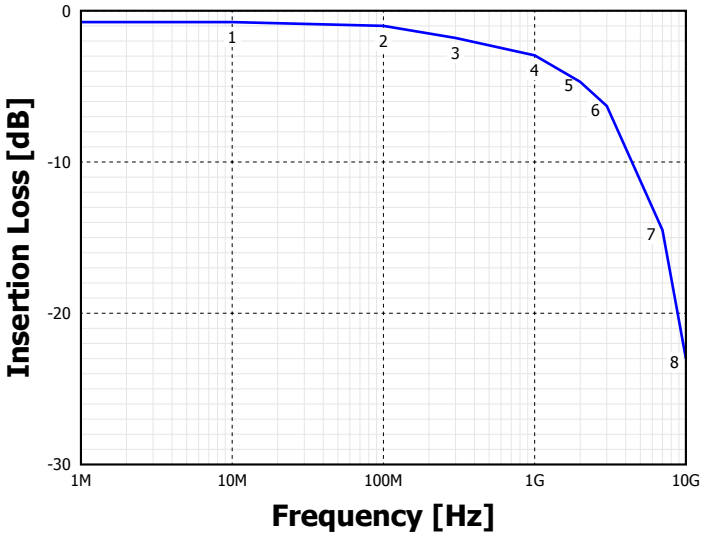


Point	f [MHz]	Loss [dB]
1	70	-0.9
2	281	-1.7
3	562	-2.6
4	1000	-4.2
5	2000	-7.6
6	4000	-13.0
7	6000	-25.0

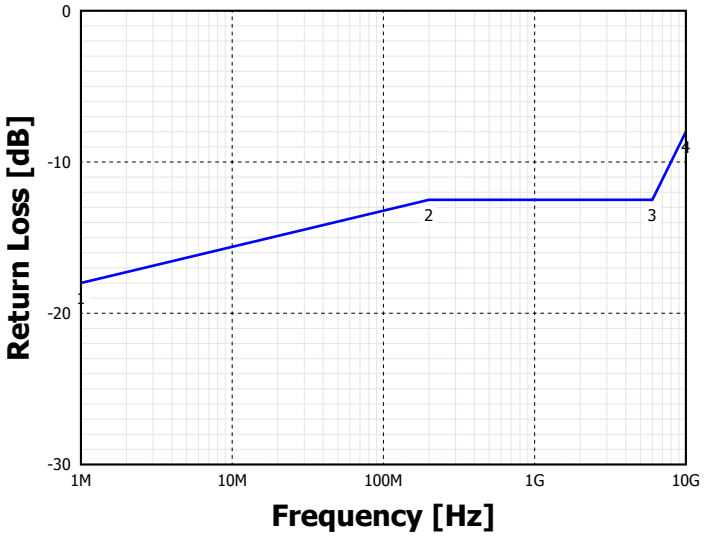


Point	f [MHz]	Loss [dB]
1	100	-19
2	2000	-3
3	6000	-3

Figure 3.26: System Board Insertion and Return Loss Requirements TMDS/HDMI $\leq$ 225MHz



Point	f [MHz]	Loss [dB]
1	10	-0.75
2	100	-1.0
3	300	-1.8
4	1000	-2.95
5	2000	-4.7
6	3000	-6.3
7	7000	-14.5
8	10000	-23.0



Point	f [MHz]	Loss [dB]
1	1	-18
2	200	-12.5
3	6000	-12.5
4	10000	-8.0

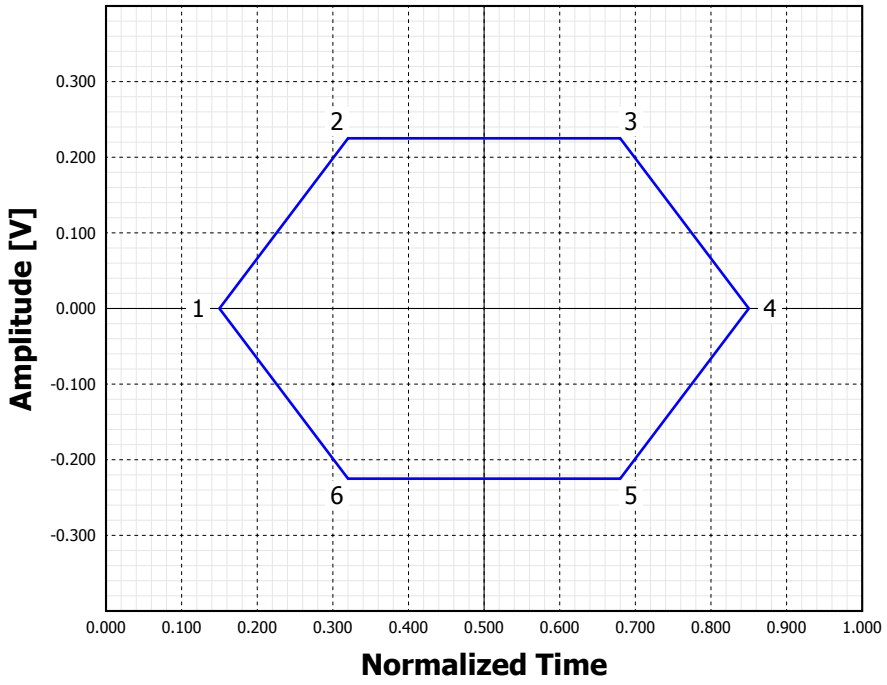
Figure 3.27: System Board Insertion and Return Loss Requirements for HDMI > 225MHz

3.5.5 LVDS

The LVDS port on the MXM module must meet the specification in Table 3.29 and Figure 3.28.

Table 3.29: Module Specifications for LVDS

Symbol	Parameter	Min	Max	Unit
$T_{SKEW-INTER-M}$	Inter-pair skew		500	ps
$T_{SKEW-INTRA-M}$	Intra-pair skew		100	ps
T_{RISE}/T_{FALL}	Rise/Fall times		1500	ps
V_{os}	Common mode voltage	1.115	1.365	V
V_t	Single ended swing level	245	455	mV
	Overshoot/Undershoot (differential)		20	%

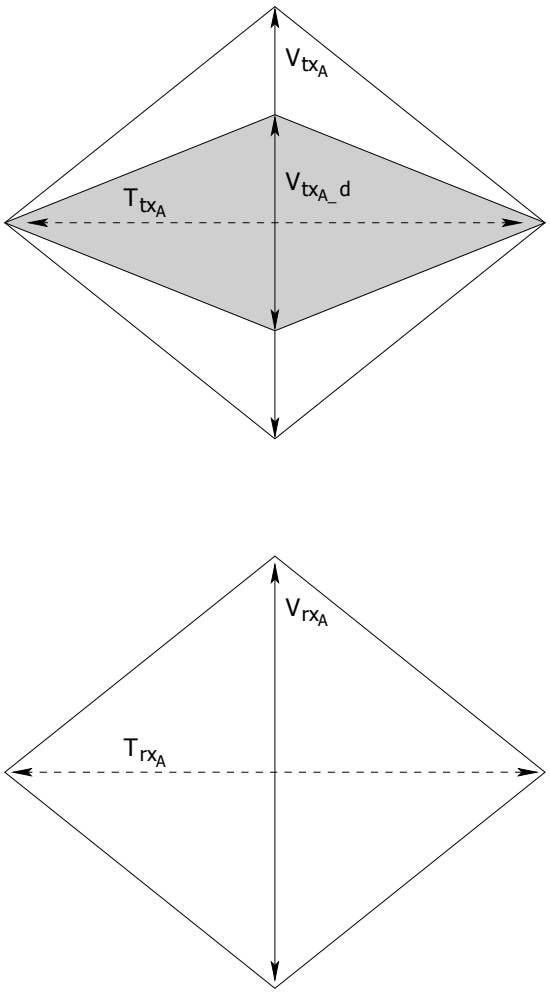


Point	X	A [V]
1	0.150	0.000
2	0.320	0.225
3	0.680	0.225
4	0.850	0.000
5	0.680	-0.225
6	0.320	-0.225

Figure 3.28: LVDS TP_MXM Eye Diagram

3.5.6 PCI Express

Figure 3.29 shows the eye diagram requirement for the MXM module validation. The specification assumes an ideal reference clock without jitter and all links active while generating the eye diagram. An MXM module that supports 8 GT/s must meet the eye requirement on each lane with one or more transmit equalization presets.



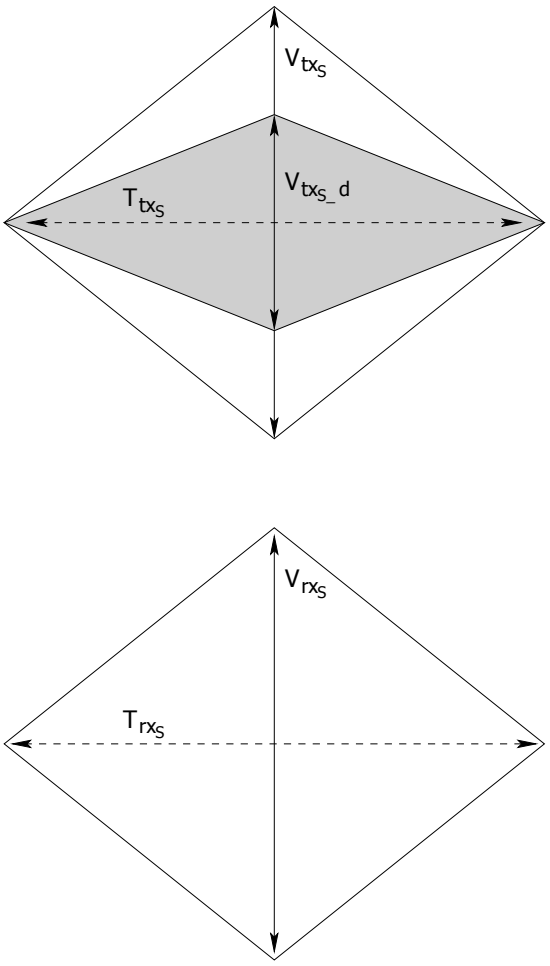
Parameter	Gen1		Gen2			Unit
Link Speed	2.5	2.5	5	5	5	GT/s
Swing	Low	Full	Low	Full	Full	
de-emphasis	0	-3.5	-3.5	-3.5	-6	dB
V_{tx_A}	262	466	170	340	300	mV
$V_{tx_A\_d}$	N/A	314	170	340	260	mV
T_{tx_A}	254	254	123	123	123	ps
Deterministic Jitter (Dj)			57	57	57	ps
Total Jitter (Tj)			77	77	77	ps

Parameter	Gen3 TX			Unit
Link Speed	8	8	8	GT/s
Swing	RS50	RS25	Full	
DFE	Off	Off	Enabled	
TXEQ preset	P1, P3, P5		P1, P7, P8	
V_{tx_A}	59	63	34	mV
T_{tx_A}	42.88	40.5	41.25	ps

Parameter	Gen3 RX		Unit
Link Speed	8	8	GT/s
Swing	RS	Full	
DFE	Off	Enabled	
TXEQ preset	N/A	N/A	
V_{rx_A}	63	34	mV
T_{rx_A}	42.88	41.25	ps

Figure 3.29: MXM Module Transmitter and Receive Compliance Eye Diagram

Figure 3.30 shows the eye diagram requirement for the system validation. The specification assumes an ideal reference clock without jitter and all links active while generating the eye diagram. A system that supports 8 GT/s must meet the eye requirement on each lane with one or more transmit equalization presets determined by the measured ps21 equivalent, Table 3.30, at the end of the system board channel. For system receive calibration, each channel classification is determined by PS21 equivalent testing, then the source is calibrated using the matching system model. The receiver is then tested with the calibrated source, using the behavioral model from Table 3.30 in the analyzer.



Parameter	Gen1		Gen2			Unit
Link Speed	2.5	2.5	5	5	5	GT/s
Swing	Low	Full	Low	Full	Full	
de-emphasis	0	-3.5	-3.5	-3.5	-6	dB
V_{tx_S}	216	232	170	200	200	mV
$V_{tx_S\_d}$	N/A	223	170	200	200	mV
T_{tx_S}	242	242	95	95	95	ps
Deterministic Jitter (Dj)			57	57	57	ps
Total Jitter (Tj)			105	105	105	ps

Parameter	Gen3 TX		Unit
Link Speed	8	8	GT/s
Swing	RS	Full	
DFE	Off	Enabled	
V_{tx_S}	63	34	mV
T_{tx_S}	42.88	41.25	ps

Parameter	Gen3 RX			Unit
Link Speed	8	8	8	GT/s
Swing	RS50	RS25	Full	
DFE	Off	Off	Enabled	
V_{rx_S}	59	63	34	mV
T_{rx_S}	42.88	40.5	41.25	ps

Figure 3.30: System Board Transmit and Receive Path Compliance Eye Diagram

Table 3.30: System Board 8 GT/s Channel Classification

Parameter	Channel				Unit
System ps21 minimum loss	0	6.9	9.4	12	dB
8 GT/s TXEQ Preset	P1, P3, P5		P1, P7, P8	P7, P8	
PEX_STD_SW# Pull-Down Resistor	No Connect	147	7.15	0	kΩ
System Model for RX Calibration	RS50	RS25	Full	Full	
Channel Classification	Short	Medium Short	Medium Long	Long	
Recommended Swing Setting for PCIe Gen1 and Gen2	Low	Low	Full	Full	

3.6 DC Specifications

Table 3.31: CMOS and Open Drain Signals DC Specifications

Symbol	Parameter	Conditions	Min	Max	Units
CMOS Outputs					
V_{OL}	Output Low Voltage	I_{out} = 8 mA		0.3	V
V_{OH}	Output High Voltage	I_{out} = -8 mA	V_{3V3}-0.3		V
I_{out}	Output Current	V_{3V3} = 3.3 V	-8	8	mA
Open Drain Outputs					
V_{OL}	Output Low Voltage	I_{out} = 8 mA		0.3	V
I_{sink}	Sink Current			8	mA
PEX_RST# and PWR_LEVEL Inputs					
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{3V3}+0.5	V
C_{in}	Input Capacitance			30	pF
I_{in}	Input Leakage Current	0 to 3.3 V	-100	100	µA
All other CMOS Inputs					
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{3V3}+0.5	V
I_{in}	Input Leakage Current	0 to 3.3 V	-1	1	mA
Open Drain Inputs					
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{3V3}+0.5	V

Chapter 4

Thermal Specification

The MXM version 3.1 thermal and mechanical specifications enable interchangeability of MXM graphics modules from alternate manufacturers with a single thermal solution. A notebook system integrator will be able to design a single thermal solution and be assured that it is mechanically and thermally compatible with all MXM graphics modules provided the module is also MXM version 3.1 compliant and of the same or lower Total Graphics Power (TGP). An example of this interchangeability concept is presented in Figure 4.1.

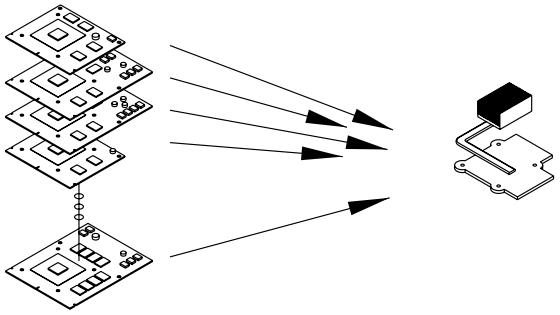


Figure 4.1: MXM Thermal Compatibility

4.1 Thermal Specification Philosophy

The thermal specification utilizes definitions of thermal regions with known graphics subsystem power to impose thermal constraints on the computer system, MXM module (PCB and Components), and the thermal solution that enables the MXM version 3.1 concept of one cooler for multiple boards.

4.1.1 System Thermal Components

A MXM compliant computer system, from a thermal perspective, can be subdivided into three separate components:

- ❑ MXM module
- ❑ System housing
- ❑ Thermal solution

The three components are shown graphically in Figure 4.2.

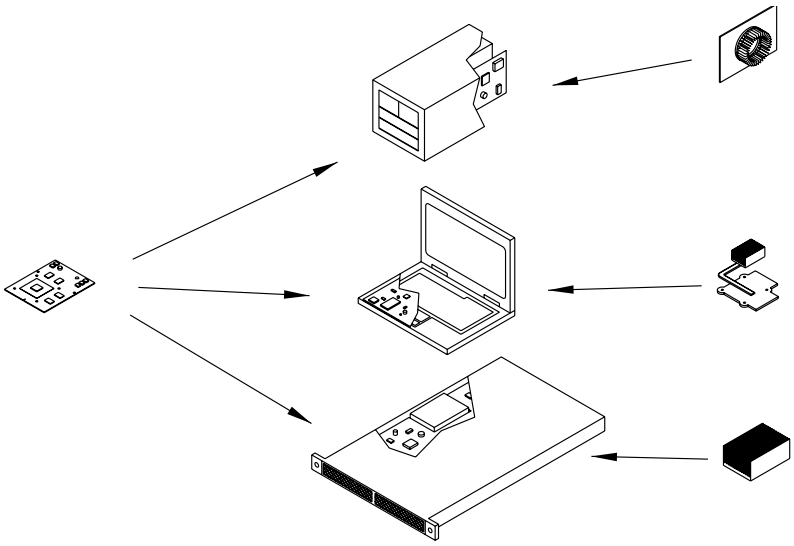


Figure 4.2: MXM System Thermal Components

The MXM version 3.1 specification defines distinct requirements on each of these three components. The MXM module component is defined by a thermal budget based on the maximum allowable temperatures of all non-GPU components. The system housing requirements are defined by an ambient temperature restriction. The thermal solution component is specified by temperatures on the heat spreader/thermal plate as well as the overall TGP.

4.1.2 Power Sources

A key part of deriving the thermal specification is having an understanding of the amount of power that each component on the graphics board will dissipate. Components are grouped into two types. A group that requires direct cooling and a group that does not. All components that require direct cooling must only be placed on the top side of the MXM module in one of the three thermal zones defined in Figure 4.6 for Type-A and Figure 4.7 for Type-B. The manufacturer's data sheets should be consulted to make a placement assessment in conjunction with the typical power distribution breakdown given in Table 4.1. The power dissipated per component will vary significantly depending on the total board power. However, the distribution of power between power consuming components is relatively constant and even when the distribution does vary, the changes will primarily impact spreading resistance in the cooler plate rather than overall cooling capacity.

Table 4.1: MXM Assumptions on Power Distribution

Component/Group	Zone	% of Module TGP
GPU	1	70 ± 5
Memory	2	17 ± 5
Power Supply	3	17 ± 5

Note: The sum of the power split described in Table 4.1 intentionally exceeds 100%. The resulting extra 4% is to account for a small spreading resistance overdesign to ensure compatibility across multiple boards utilizing different memory technologies.

4.2 Thermal Requirements

4.2.1 Module Thermal Requirements

It is the responsibility of the board designer to assess whether components will be adequately cooled on the board given the guidance from the MXM specification. The MOSFETs and inductors also have clearly defined maximum operational limits on which the system integrator can impose additional deratings if they so choose. To ensure proper placement and height considerations, the module designer shall always be fully responsible for specifying the thermal interface material needed to cool board components. Thermal interface materials must be selected such that when the thermal solution is mounted to the MXM module that there is no deflection beyond allowable mechanical limits specified in the MXM version 3.1 specification, Section 2.3.3. The module designer must select interface materials for all non-GPU components given the two sets of bounding temperatures and the power distribution estimates obtained using Table 4.1 and Table 4.4. In all situations except what is outlined in the following paragraph, the non-GPU thermal interface pads shall accompany the MXM module and be part of the BOM of the MXM module.

The only exception to the above requirement is if a system integrator has adequate control over the graphics board design and supply chain such that the integrator can manage the acquisition and assembly of the interface material separately from the board acquisition. However, even if the system integrator assumes responsibility for thermal interface material acquisition and assembly, the graphics board supplier is still responsible for specifying the interface material. After the system has been assembled, and if an MXM board is to be replaced with a new module, then the thermal interface materials for that new board must accompany that replacement MXM module.

The memory is a special case because there will be designs that require memory to be on the back of MXM modules. The memory on the top will be cooled directly by the thermal solution, and the memory on the back will not have any direct cooling. In both the cooled and uncooled case, the maximum allowable memory case temperature is 115 °C.

Note: Components requiring direct cooling are not allowed on the back side of the PCB.

4.2.2 System Requirements

The system requirements are summarized in Table 4.2. The internal ambient temperatures near the module are measured from the locations near the bottom of the MXM PCB shown in Figure 4.3. The maximum allowable average temperature is 65 °C, and the highest of any of the three must be less than or equal to 75 °C. The height of the temperature measurement locations is 4 mm from the bottom of the MXM module. If the required clearance is not available because of mechanical assembly (for example the system board or the system chassis are closer than 4 mm from the module), then the temperature of the surface adjacent to the module should be measured.

Table 4.2: Ambient Temperature Specification

Internal Average Ambient Temperature	$T_{A(avg)} = (T_{A1}+T_{A2}+T_{A3})/3 \leq 65\,°C$
Internal Individual Ambient Temperature	$(T_{A1},T_{A2},T_{A3}) \leq 75\,°C$

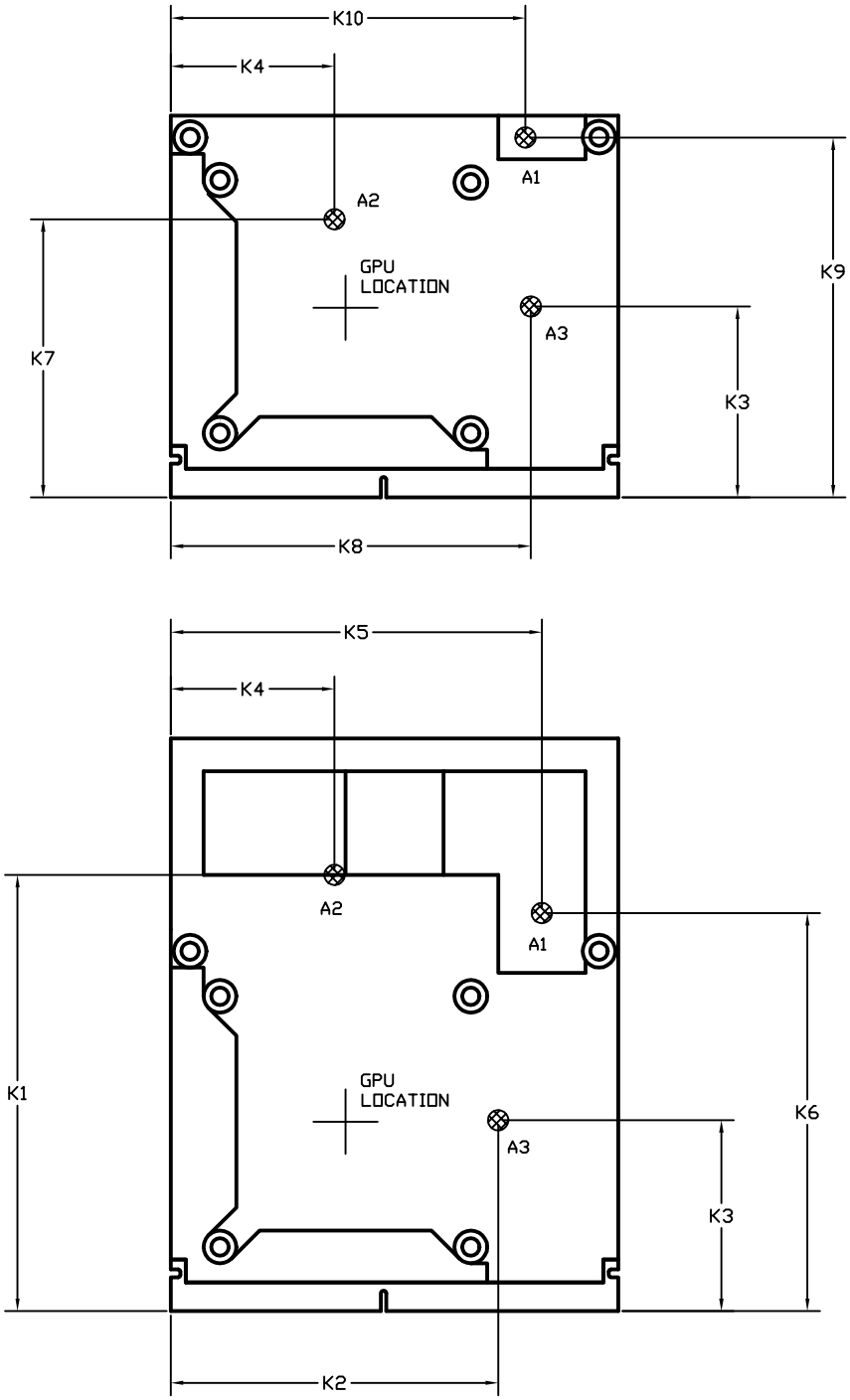


Figure 4.3: Type A and Type B Ambient Temperature Measurement Locations

Table 4.3: Ambient Temperature Measurement Locations Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
K1	79.74	80.00	80.26	3.139	3.150	3.160
K2	59.74	60.00	60.26	2.352	2.362	2.372
K3	34.74	35.00	35.26	1.368	1.378	1.388
K4	29.74	30.00	30.26	1.171	1.181	1.191
K5	67.74	68.00	68.26	2.667	2.677	2.687
K6	72.74	73.00	73.26	2.864	2.874	2.884
K7	50.74	51.00	51.26	1.998	2.008	2.018
K8	65.74	66.00	66.26	2.588	2.598	2.609
K9	65.74	66.00	66.26	2.588	2.598	2.609
K10	64.74	65.00	65.26	2.549	2.559	2.569

4.2.3 Thermal Solution Requirements

The thermal solution for the MXM version 3.1 graphics board includes the GPU thermal interface material, thermal spreader, heat transport mechanism and heat exchanger to the external ambient thermal sink. The cooler shall maintain all critical component temperatures below their maximum values. The mechanical attachment of the cooler shall be GPU die referenced with center loading. All non-GPU thermal interface material is part of the MXM module as described in Section 4.2.1. The thermal conditions outlined in the specification must be met with no forced air flow across the MXM PCB. It is left to the system and thermal solution designers to determine appropriate external ambient and/or fan inlet temperatures based on their respective design criteria.

Note: Regardless of the operational mode of the MXM module, all board components shall not exceed the derated critical temperatures set by the MXM module designer and secondarily, the manufacturer's temperature limits.

The spreading capability of the thermal solution is assured by maintaining required temperatures within each of three thermal spreader zones. These zones are shown in Figure 4.6 and Figure 4.7. Zone 1 is for the GPU, Zone 2 is for the memory, Zone 3 for the power supply. It is highly recommended that MOSFETs for the power supply be located along the periphery of the power supply zone for Type-B in the 1.5 mm PCB keep-in zone to ensure the best possible cooling.

The temperature of a specific thermal zone must meet the temperature requirements defined in Table 4.4 while keeping each component within their respective thermal limits. In order to meet or exceed the minimum thermal requirements, the thermal solution designer has the flexibility to customize the cooler provided that the temperature limits are met and the physical height restrictions on the MXM module are respected.

Table 4.4: Maximum Spreader Plate Temperatures

Component/Group	Zone	Symbol	Maximum Temperature
GPU	1	T_1	90 °C
Memory	2	T_2	90 °C
Power Supply	3	T_3	90 °C

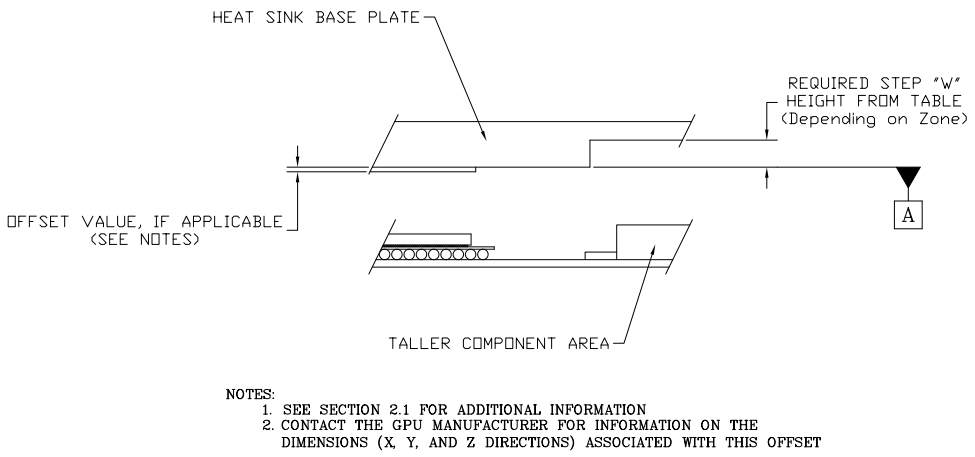


Figure 4.4: Bottom Side Profile Steps

The cooler spreader plate must maintain a specific profile to preserve the physical compatibility with different MXM modules and ensure optimal thermal interface material selection.

The cooler profile requirements are described in Table 4.5 and Figure 4.4. These requirements only apply to the bottom of the spreader. There are no restrictions for the top side of the spreader. The first column references the PCB top side height restrictions described in Figure 2.5 and Figure 2.6. The second column describes the cooler profile in terms of the step increases away from the PCB relative to the 1.5 mm board height zone which is used as a plane datum for the step increases.

The keep-out definitions described in Section 2.4 are for board level components. An additional 0.5 mm of clearance spacing is required from the thermal solution contact plate. This 0.5 mm thermal plate offset is spaced in the x and y direction and provides a minimum clearance, under any tolerance conditions, between the thermal plate and board level components. Refer to Figure 4.5 for details.

Table 4.5: Thermal Solution Spreader Bottom Side Profile Step Requirements

Top Side Height Restriction	Spreader Plate Profile Requirement (W)
1.5 mm	Base Height (Datum)
1.8 mm	+0.6 mm Step
2.2 mm	+1.0 mm Step
4.0 mm	+2.8 mm Step

Note: Tolerance for the step heights in Table 4.5 is +0.1/-0.0 mm

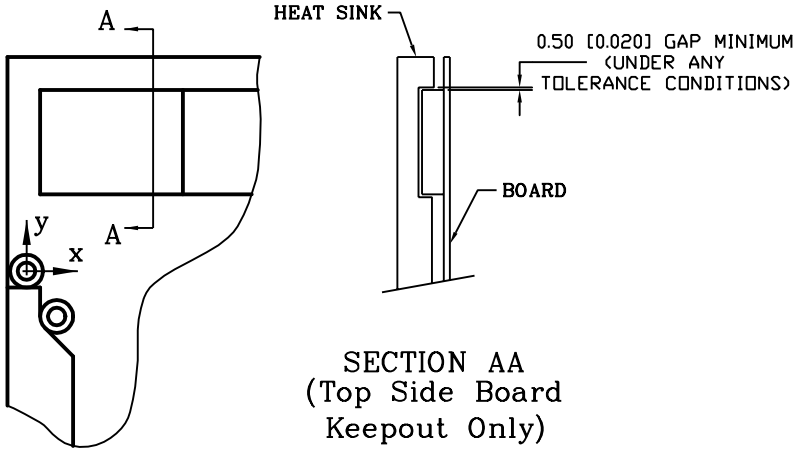


Figure 4.5: Bottom Side Profile Component Clearance

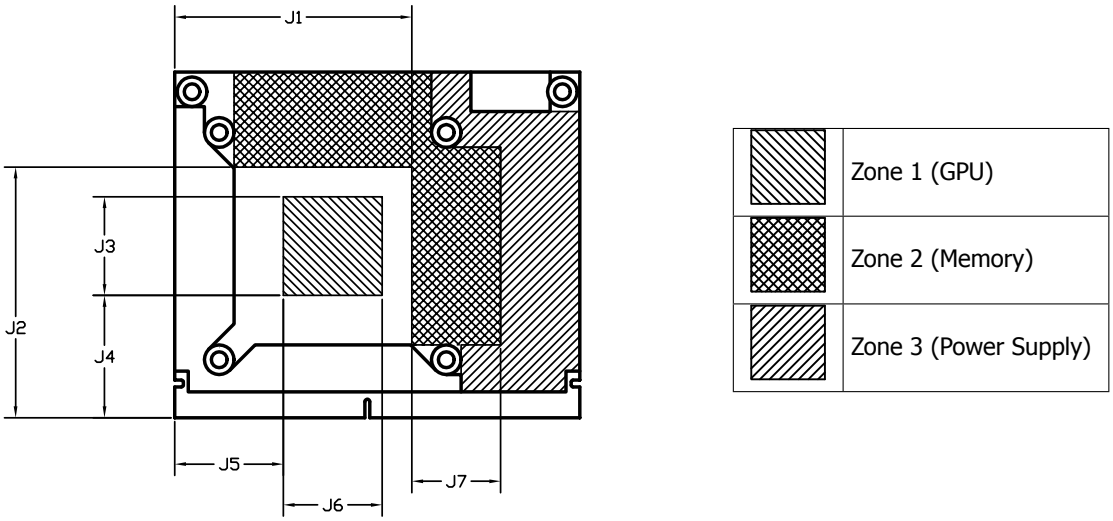


Figure 4.6: Type A Thermal Zones

Table 4.6: Type A Thermal Zones Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
J1	47.87	48.00	48.13	1.885	1.890	1.895
J2	50.62	50.75	50.88	1.993	1.998	2.003
J3	19.87	20.00	20.13	0.782	0.787	0.793
J4	24.62	24.75	24.88	0.969	0.974	0.980
J5	21.87	22.00	22.13	0.861	0.866	0.871
J6	19.87	20.00	20.13	0.782	0.787	0.793
J7	18.00	18.00	18.00	0.709	0.709	0.709

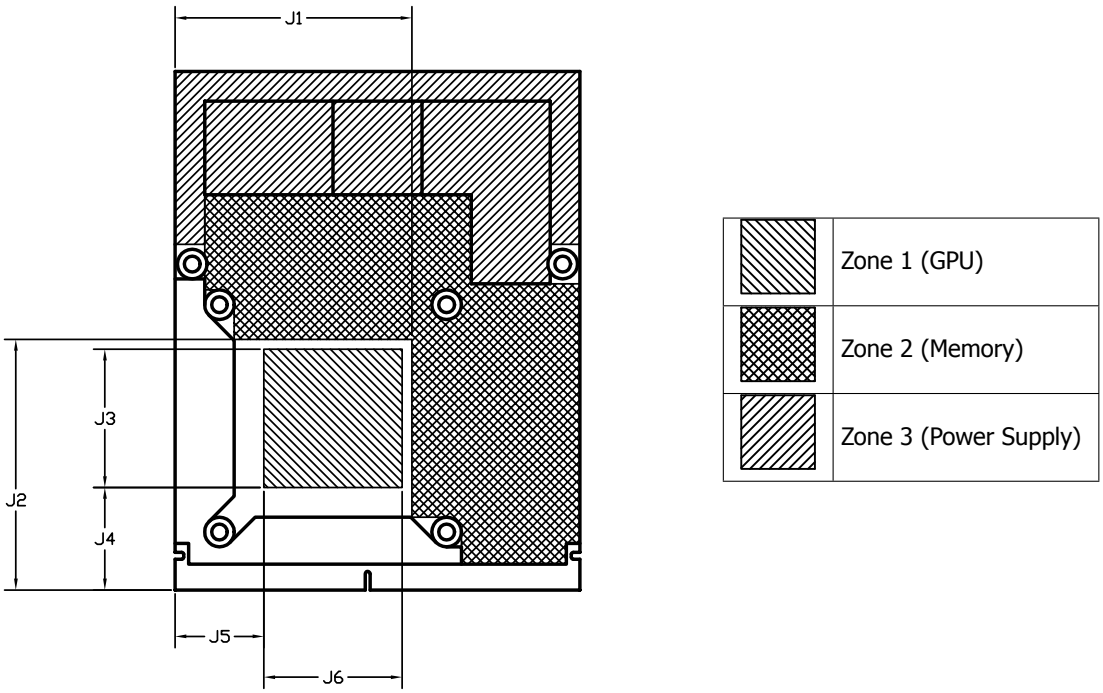


Figure 4.7: Type B Thermal Zones

Table 4.7: Type B Thermal Zones Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
J1	47.87	48.00	48.13	1.885	1.890	1.895
J2	50.62	50.75	50.88	1.993	1.998	2.003
J3	27.87	28.00	28.13	1.097	1.102	1.107
J4	20.62	20.75	20.88	0.812	0.817	0.822
J5	17.87	18.00	18.13	0.704	0.709	0.714
J6	27.87	28.00	28.13	1.097	1.102	1.107

4.3 Thermal Specification Summary

The MXM Thermal specification is summarized in Table 4.8. The specification makes specific assumptions described in Table 4.1 on the power distribution on the module. Refer to the appropriate sections for detailed explanations.

Table 4.8: Thermal Specification Summary

Thermal Region	Specification	Notes
System	$T_{A(avg)} \leq 65\,°C$	The average temperature of three locations (Section 4.2.2).
System	$(T_{A1},T_{A2},T_{A3}) \leq 75\,°C$	Maximum temperature at any of the locations.
Memory	$T_{Case} \leq 115\,°C$	For memory on the front or back side.
Zone 1	$T_1 \leq 90\,°C$	Temp. of spreader directly above the GPU (Section 4.2.3).
Zone 2	$T_2 \leq 90\,°C$	Temp. of spreader in the zone over the memory (Section 4.2.3).
Zone 3	$T_3 \leq 90\,°C$	Temp. of spreader in the power supply zone (Section 4.2.3).

Applicable Documents

The following documents contain provisions which through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. However, users of this standard are advised to ensure they have the latest versions of referenced standards and documents.

- *MXM Graphics Module Software Specification*, Version 3.0, Revision 1.1
- *MXM Version 3.0 System Design Guide*, Revision 1.0
- *MXM Version 3.0 Mechanical Design Guide*, Revision 1.1
- *MXM Version 3.0 Thermal Design Guide*, Revision 1.1
- *MXM Version 3.0 Graphics Module Tolerance Analysis and Design Suggestions*, Revision 1.0
- *MXM Version 3.0 Connector Interoperability Design Guide*, Revision 1.1
- *PCI Express Base Specification*, Revision 3.0
- *PCI Express Card Electromechanical Specification*, Revision 3.0
- *VESA DisplayPort Standard*, Version 1, Revision 2
- *VESA DisplayPort Interoperability Guideline*, Version 1.1
- *VESA Embedded DisplayPort (eDP)*, Version 1.2
- *VESA Enhanced Display Data Channel (EDDC) Standard,* Version 1.2
- *SMBus Specification*, Revision 2.0
- *Advanced Configuration and Power Interface (ACPI) Specification*, Revision 3.0b
- *SPWG Notebook Panel Specification*, Version 3.0
- *Digital Visual Interface (DVI)*, Version 1.0
- *HDMI 1.4 – High-Definition Multimedia Interface (HDMI) Specification*
- *JTAG Specification (IEEE 1149.1)*
- *IPC-A-600F – Acceptability of Printed Circuit Boards*
- *IPC-A-610D – Acceptability of Electronic Assemblies*
- *EIA-364-9 – Durability Test Procedure for Electrical Connectors and Contacts*
- *EIA-364-28D – Vibration Test Procedure for Electrical Connectors and Sockets*
- *EIA-364-27B – Mechanical Shock (Specified Pulse) Test Procedure for Electrical Connectors*
- *EIA-364-23B – Low Level Contact Resistance Test Procedure for Electrical Connectors and Sockets*
- *EIA-364-13C – Mating and Unmating Forces Test Procedure for Electrical Connectors*
- *EIA-364-21C – Insulation Resistance Test Procedure for Electrical Connectors, Sockets and Coaxial Contacts*
- *EIA-364-20C – Withstanding Voltage Test Procedure for Electrical Connectors, Sockets and Coaxial Contacts*

- *EIA-364-108 – Impedance, Reflection Coefficient, Return Loss and VSWR Measured in the Time and Frequency Domain Test Procedure for Electrical Connectors, Cable Assemblies or Interconnection Systems*
- *EIA-364-101 – Attenuation Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems*
- *EIA-364-90 – Crosstalk Ratio Test Procedures for Electrical Connectors, Sockets, Cable Assemblies or Interconnect Systems*
- *EIA-364-1000.1 – Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications*
- *ASME Y14.5M – Dimensioning and Tolerancing Standard*

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