LEC-BW

(Low Energy Computer On Module)

Technical Reference

P/N 50-1Z206-1010

Rev 2.00

STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

Advance Technologies. Automate the World.

Preface

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Revision History

Revision	Date	Description of Change(s)
1.00	06/08/2016	Initial Release
2.00	12/02/2016	Removed Standby voltage from Table 1-3 on page 4; added mounting information to cooling section in Chapter 1; added Ordering Information to Chapter 1

Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

Environmental Responsibility

ADLINK is committed to fulfill its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

Important Safety Instructions

For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information.

This information adds clarity or specifics to text and illustrations.

This information indicates the possibility of ***minor*** physical injury, component damage, data loss, and/or program corruption.

This information warns of possible ***serious*** physical injury, component damage, data loss, and/or program corruption.

Table of Contents

1 Product Overview

1.1 Description

The LEC-BW Computer-On-Module (COM) combines the SMARC® 1.1 standard with the Intel® Pentium® and Celeron® N-series System-on-Chip (SoC), providing an ideal solution for low power consumption and high performance requirements. The module provides the high integration, high performance, low power, and ruggedness favored by Internet-of-Things (IoT) applications such as retail transactional clients, digital signage, and in-vehicle infotainment systems.

The LEC-BW module utilizes the Intel N3000 series SoC, which is based on the new Intel Architecture and is manufactured on Intel's industry-leading, tri-gate 14nm process. The module primarily targets entry-level 2-in-1 devices, lap tops, desktops, and all-in-one PCs and supports contemporary, high-bandwidth interfaces such as Ultra HD HDMI, PCI Express Gen2, Gigabit Ethernet, USB 3.0, SATA Gen3, and a state-of-the-art HD Audio interface. The module generates its own LVDS (18/24bit), TMDS, and Display Port video signals using DDI output from the SoC.

Two SPI Flash chips implement a fail-safe BIOS, allowing the user to boot the module even if current BIOS settings have corrupted the system.

Under the management of the BMC chip (Board Management Controller), the SEMA utility (Smart Embedded Management Agent) provides system control, security, and failure protection—counting, monitoring, and measuring hardware and software events, and using the SMBus to send corrective commands to the SoC. The optional SEMA Cloud utility not only controls local events on the module but system client events on the IoT.

1.2 Features

CPU

Intel® Pentium® and Celeron® N-Series, x86 dual-core or quad-core SoC (System On Chip) with integrated memory, graphics, and I/O. See Intel website.

- N3710 6W TDP, Pentium Quad-Core/2.56GHz burst freq./1600 MT/s /Gfx 700MHz
- N3160 6W TDP, Celeron Quad-Core/2.24GHz burst freq./1600 MT/s/Gfx 640MHz
- N3060 6W TDP, Celeron Dual-Core/2.48GHz burst freq./1600 MT/s/Gfx 600MHz
- N3010 4W TDP, Celeron Dual-Core/2.24GHz burst freq./1600 MT/s/Gfx 600MHz
- x5-E8000 5W TDP, Atom Quad-Core/2.00GHz burst freq./1600 MT/s/Gfx 320MHz

NOTE: Other CPU SKUs can be made available on request.

- Memory
  - Up to 8GB non-ECC, unbuffered soldered, DDR3L
  - 1600MHz
  - Single channel
- Interface Standard
  - SMARC, board-to-board, Rev 1.1
- SATA
  - Two 6Gb/s, Gen 3 ports
  - Advanced Host Controller Interface (AHCI)
- USB
  - Four USB 2.0 host ports
  - One USB 3.0 host port on AFB
- Ethernet
  - Single-port, gigabit Ethernet controller
  - Integrated GbE MAC, PHY, and MDI ports
  - 10T/100TX/1000T signals using the PCIe x1 bus
- Serial UART
  - One high-speed, 2-wire port
  - One high-speed, 4-wire port
  - Base frequency 50MHz
- I2C
  - One I2C bus
  - Four I2C ports
  - One SMBus
- SPI
  - Two internal SPI controllers
  - Two SPI flash devices for BIOS storage
- Video
  - Display Port/HDMI
  - LVDS
- Audio
  - One HDA (High Definition Audio) interface (through I2S port 2)
- Camera
  - Two MIPI-CSI camera interfaces
  - Camera, CSI0 (2 lanes)
  - Camera, CSI1 (4 lanes)

1.3 Block Diagram

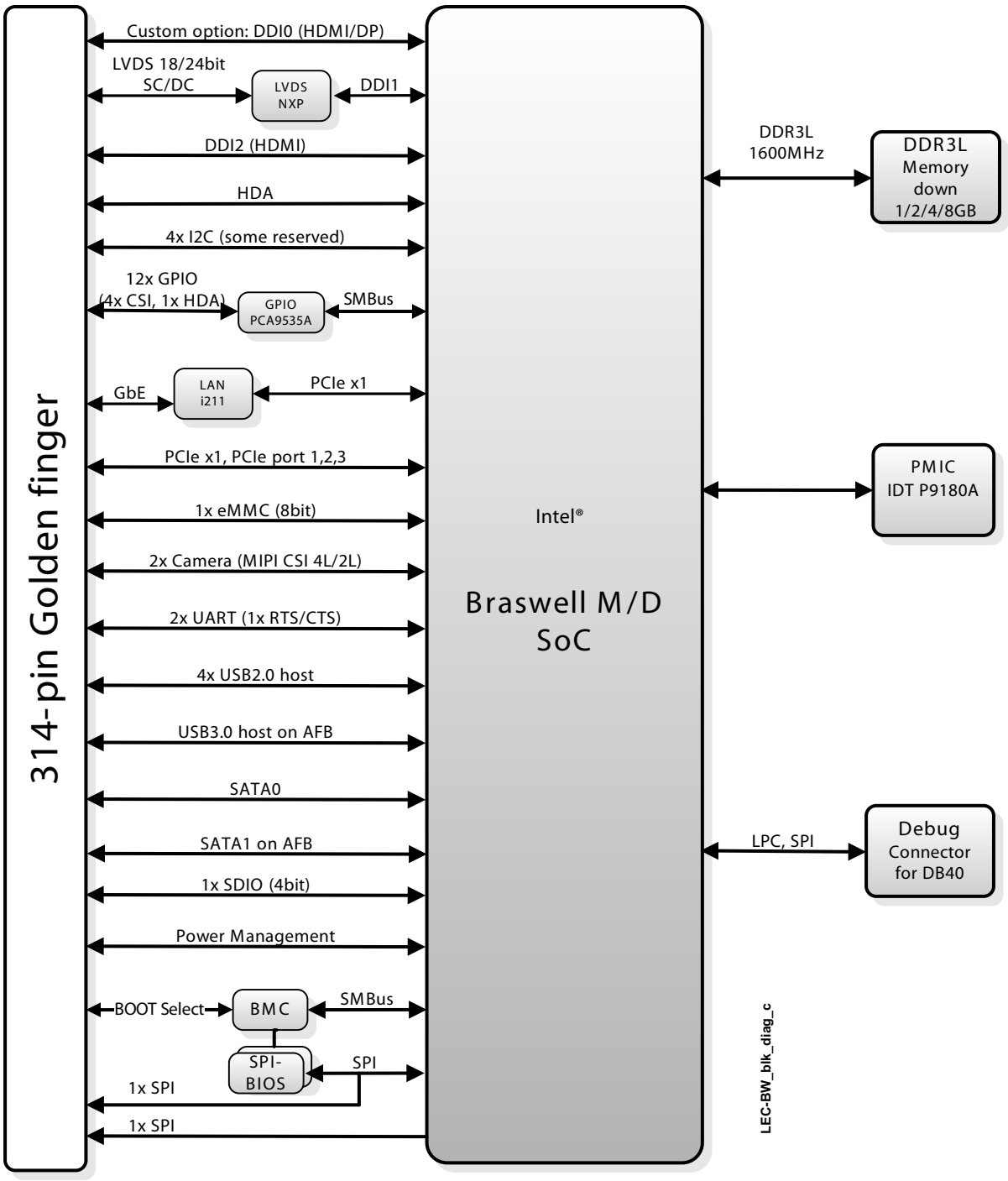


Figure 1-1: Module functional block diagram

1.4 Ordering Information

Table 1-1: LEC-BW Models

Model Number	Description
LEC-BW42-4G-CT	SMARC short size module with Intel Pentium N3710, quad core, 4GB DDR3L, 0°C to 60°C
LEC-BW41-4G-CT	SMARC short size module with Intel Celeron N3160, quad core, 4GB DDR3L, 0°C to 60°C
LEC-BW22-2G-CT	SMARC short size module with Intel Celeron N3060, dual core, 2GB DDR3L, 0°C to 60°C
LEC-BW21-2G-CT	SMARC short size module with Intel Celeron N3010, dual core, 2GB DDR3L, 0°C to 60°C
LEC-BW-HS	Heat spreader for LEC-BW
LEC-BW-HS2	Passive heatsink for LEC-BW (requires LEC-BW heat spreader)

1.5 Specifications

1.5.1 Physical

Table 1-2 lists the physical dimensions of the module.

Table 1-2: Weight and Footprint Dimensions

Dimension	Measurement	
Weight	0.020 kg [0.089 kg with heat spreader]	Overall height is measured from the upper board surface to the top of the highest permanent component on the upper board surface. This measurement does not include the cooling solution.
Height (overall)	2.29mm	
Board thickness	1.20mm	
Width	50.00mm	
Length	82.00mm	

1.5.2 Electrical

Table 1-3 specifies the electrical characteristics of the module.

Table 1-3: Electrical Specifications

Parameter	Value
Voltage Input Standard RTC	▶ +3V DC min to +5.25V DC max, +/-5%, =/- 50mV ripple ▶ 3.0V, 2.0V to 3.3V (battery), +/- 20mV ripple
Power States	▶ C0, C1, C2 processor power states ▶ S0 (active), S1 (sleep), S2 (extended sleep), S3 (standby [suspend to RAM]), S4 (suspend-to-disk), and S5 (soft-off and wake-on-LAN) system power states

1.5.3 Environmental

Table 1-4 defines the environmental conditions under which the module is qualified to operate and to be stored.

Table 1-4: Temperature and Humidity

Parameter	Temperature
Temperature	
Standard	▶ 0°C to +60°C
Storage	▶ -55°C to 85°C
Humidity	
Operating	▶ 5% to 90% relative humidity, non-condensing
Non-operating	▶ 5% to 95% relative humidity, non-condensing

Table 1-5 provides shock and vibration tests performed on the board.

Table 1-5: Shock and Vibration

Parameter	Result
Shock Test	MIL-STD-202F, Method 213B, Table 213-I, Condition A
Random Vibration Test	MIL-STD-202F, Method 214A, Table 214-I, Condition D

Table 1-6 presents the average times between system failures.

Table 1-6: Mean Time Between Failures

Parameter	Value
MTBF at 40°C	490,000 hrs (according to MIL calculation)

1.5.4 Mechanical

Figure 1-2 provides the mechanical dimensions of the LEC-BW.

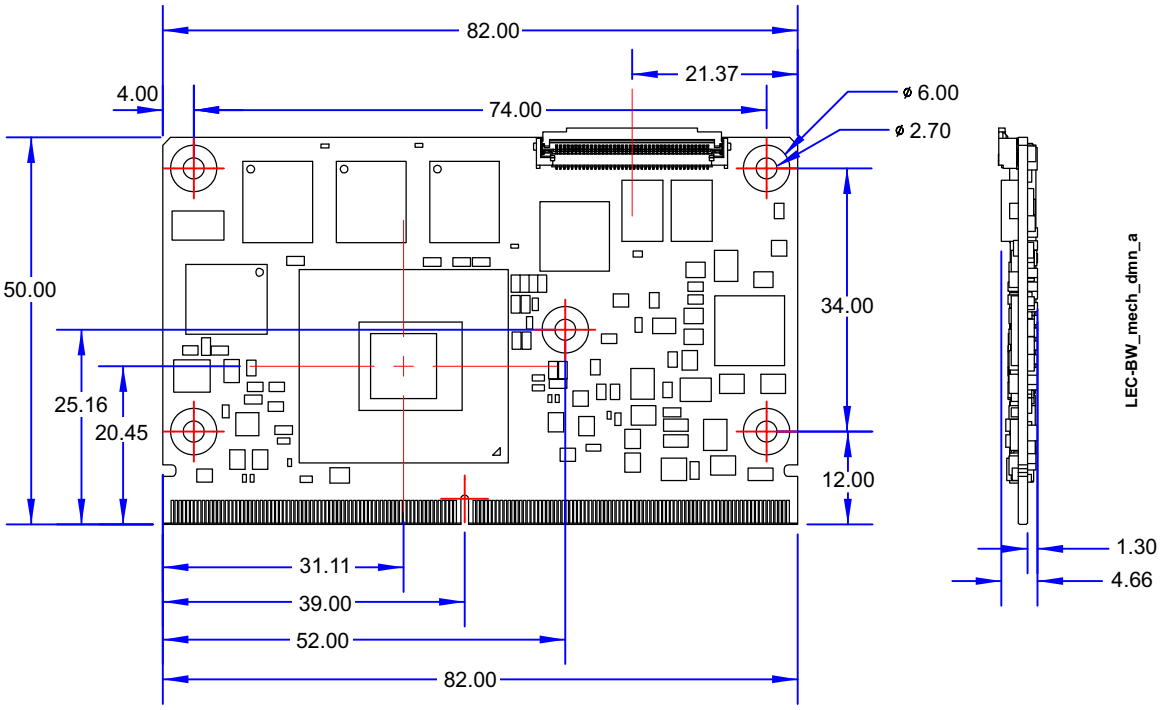


Figure 1-2: Mechanical dimensions (top side)

1.5.5 Power

Table 1-7 provides the power requirements for this module under certain load configurations.

Table 1-7: Power Supply Requirements

Parameter	6W, N3710 SoC with 4GB SDRAM, 2M cache up to 2.56 GHz	6W, N3160 SoC with 4GB SDRAM, 2M cache up to 2.24 GHz	6W, N3060 SoC with 2GB SDRAM, 2M cache up to 2.48 GHz	4W, N3010 SoC with 2GB SDRAM, 2M cache up to 2.24 GHz	5W, x5-E8000 Atom SoC with 4GB SDRAM, 2M cache up to 2.00 GHz
Input Type	Regulated DC voltage	Regulated DC voltage	Regulated DC voltage	Regulated DC voltage	Regulated DC voltage
Typical Idle Current and Power (EIST enabled; 500GB SSD; under Windows 7)	0.45A (2.25W) @ 5V	0.42A (2.10W) @ 5V	0.45A (2.25W) @ 5V	0.45A (2.25W) @ 5V	0.45A (2.25W) @ 5V
Typical Operating Mode Current and Power (EIST enabled; 500GB SSD; under Windows 7)	1.25A (6.25W) @ 5V	1.08A (5.04W) @ 5V	0.98A (4.90W) @ 5V	0.93A (4.65W) @ 5V	1.05A (5.25W) @ 5V
Maximum Operating Mode Current and Power (EIST enabled; 500GB SSD; under Windows 7; Intel TAT tool v5.0.1022)	4.06A (20.30W) @ 5V	3.15A (15.75W) @ 5V	2.70A (13.50W) @ 5V	2.66A (13.30W) @ 5V	2.26A (11.30W) @ 5V
System S3 mode (EIST enabled; 500GB SSD; under Windows 7)	0.13A (0.65W) @ 5VSB	0.12A (0.60W) @ 5VSB	0.12A (0.60W) @ 5VSB	0.13A (0.65W) @ 5VSB	0.12A (0.60W) @ 5VSB
System S4 mode (EIST enabled; 500GB SSD; under Windows 7)	0.12A (0.60W) @ 5VSB	0.11A (0.55W) @ 5VSB	0.12A (0.60W) @ 5VSB	0.12A (0.60W) @ 5VSB	0.11A (0.55W) @ 5VSB
System S5 mode with ECO enabled (EIST enabled; 500GB SSD; under Windows 7)	0.12A (0.60W) @ 5VSB	0.11A (0.55W) @ 5VSB	0.12A (0.60W) @ 5VSB	0.12A (0.60W) @ 5VSB	0.11A (0.55W) @ 5VSB

1.5.6 Cooling

The LEC-BW is designed to operate at its maximum CPU speeds and requires a thermal solution to cool the CPU. ADLINK offers a heat spreader and a passive heatsink (separate order numbers) for cooling. The heatsink can be used for module evaluation. If a custom heatsink is used, it is recommended to connect it to the ADLINK heat spreader. This facilitates future module upgrades without the need to re-design the custom heatsink.

There is a separate order number for a heat spreader, which can be mounted on the module. The heat spreader provides a neutral plane to connect a custom heatsink solution. A passive heat sink is available for customer lab evaluation. This heatsink must be mounted on top of the heat spreader. If you want to use the heatsink, it is mandatory to also use the heat spreader.

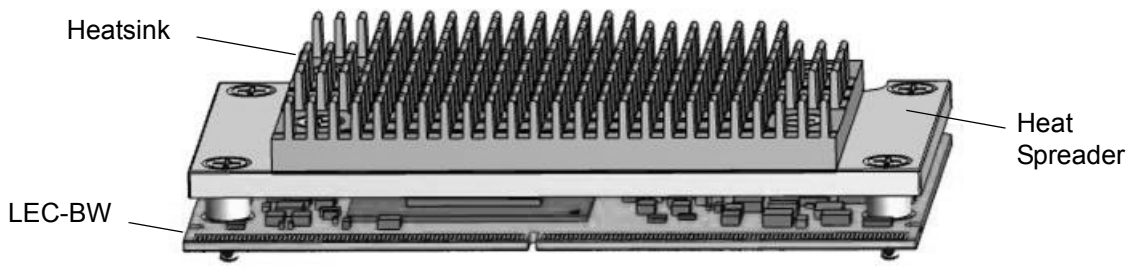
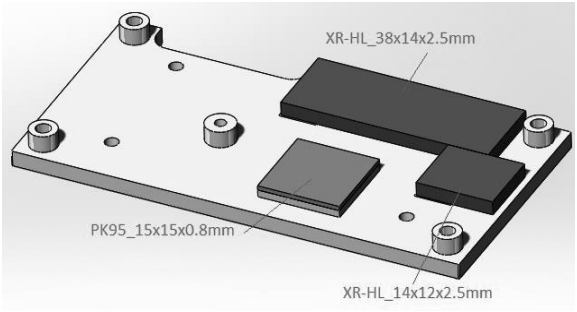


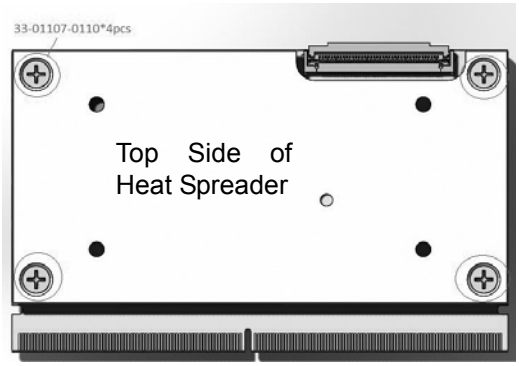
Figure 1-3: Heatsink, Heat Spreader, Module Assembly.

Cooling Solution Assembly

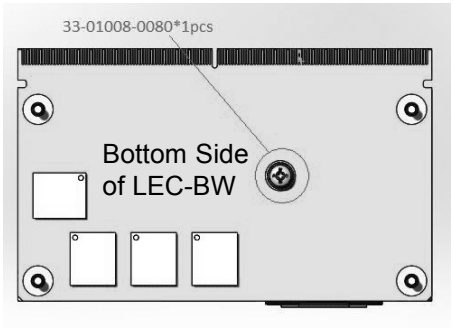
Use the following four steps to install the heat spreader and heatsink to the LEC-BW.



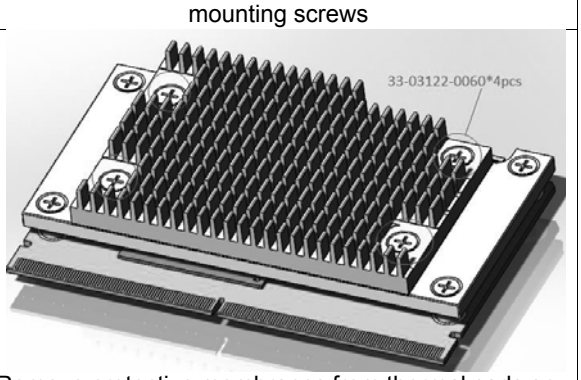
Remove protective membranes from thermal pads on the heat spreader



Mount heat spreader onto module using four M2.5x11 mounting screws



Instal one M2.5x8 mounting screw to the bottom side of the module



Remove protective membranes from thermal pads on the heatsink and mount to the heat spreader using four M3x6 mounting screws

1.6 Getting Started

Mount the LEC-BW to the carrier as illustrated in Figure 1-4, which provides a profile view of the module mounted to the carrier with dimensions.

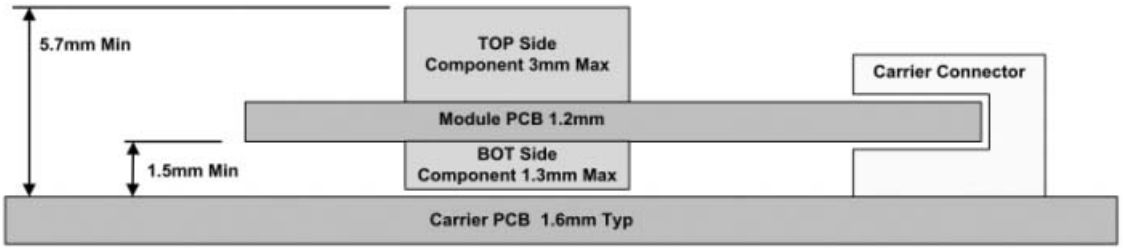


Figure 1-4: SMARC module mounting dimensions (profile)

NOTE:

ADLINK strongly recommends plastic spacers instead of metal spacers for mounting the board. Metal spacers create the possibilities of short circuits with the components located around the mounting holes, which can ruin the board.

CAUTION:

Be sure to observe the EMC security measures. Make sure you are always at the same potential as the module.

CAUTION

Never connect or disconnect peripherals like HDDs while the power supply is connected and switched on.

Use the cable set provided in the ADLINK Technology starter kit to connect the LEC-BW to a display. Connect a USB keyboard or mouse to the carrier. Use the SATA cable to connect the hard disk. Make sure that the pins match their counterparts correctly and are not twisted. If you plan to use additional peripherals, connect them to the appropriate headers or connectors on the carrier.

Connect a power supply to the power connector on the carrier and switch on the power.

NOTE:

Observe the minimum voltage values for the standard peripherals mentioned. For additional peripherals, make sure enough power is available. The system will not work if there is not enough supply current for all your devices.

The display shows the BIOS messages. If you want to change the standard BIOS settings, press the <DEL> key to enter the BIOS setup menus. See Chapter 4 for setup details.

If you need to load the BIOS default values, they can be automatically loaded at boot time.

The LEC-BW boots from CD drives, USB sticks, hard disks, or µSD-Cards. Provided that any of these is connected and contains a valid operating system image, the display then shows the boot screen of your operating system.

The LEC-BW needs adequate cooling measures depending on the desired operating temperature range. Using the board without cooling could damage the board permanently.

2 Hardware

This chapter describes the major integrated circuits (ICs) and interface connectors and headers on the module. The third section of this chapter further describes the major ICs including the manufacturers' model numbers.

2.1 Major Components (ICs)

Table 2-1 lists the major integrated circuits on the LEC-BW, including a brief description of each IC. Figure 2-1 and Figure 2-2 show the locations of the major ICs.

Table 2-1: Major Integrated Circuit Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	Intel part numbers	• N3710 Pentium (quad-core, 6W, 2.56GHz burst frequency) • N3160 Celeron (quad-core, 6W, 2.24GHz burst frequency) • N3060 Celeron (dual-core, 6W, 2.48GHz burst frequency) • N3010 Celeron (dual-core, 6W, 2.24GHz burst frequency) • x5-E8000 Atom, (quad-core, 5W, 2.00GHz burst frequency)	N-series, 14nm SoC (System on Chip) with Intel Architecture	Integrates Processor Core, Graphics / Memory Hub, and I/O Hub
Ethernet Controller (LU1 on bottom side; see Figure 2-2)	Intel	WGI211AT SLJXZ	Single-port Gigabit Ethernet controller	Integrates GbE MAC, PHY, and MDI for standard 10T/100TX/1000T Ethernet signals using the PCIe x1 bus
BMC [Board Management Controller] (BU1)	Texas Instruments	TM4C123BH6ZRB	Micro controller for board functions including Watchdog Timer, LVDS control, system control, and failure protection	Controls dual BIOS and SEMA API through the SMBus
SPI Flash (U13 and U14)	Winbond	W25Q64FVSSIG TR	Serial Peripheral Interface Flash Memory chip (for firmware)	Stores BIOS 0 and BIOS 1 in Flash Memory
DDR3L SDRAM (MD1, MD2, MD3, MD4, MD5, MD6, MD7, MD8 [MD2, MD3, MD6, and MD7 on bottom side; see Figure 2-2])	• Micron	• MT41K126M8DA-125 (1GB model) • MT41K256M8DA-125 (2GB model) • MT41K512M8DA-125 (4GB model) • MT41K1G4I (8GB model)	On-board DDR3L, 1.35V, non-ECC system memory • 4Gb, 8x 126Mx8 • 4Gb, 8x 256Mx8 • 4Gb, 8x 512Mx8 • 4Gb, 8x 1Mx8	Provides high-speed data transfer

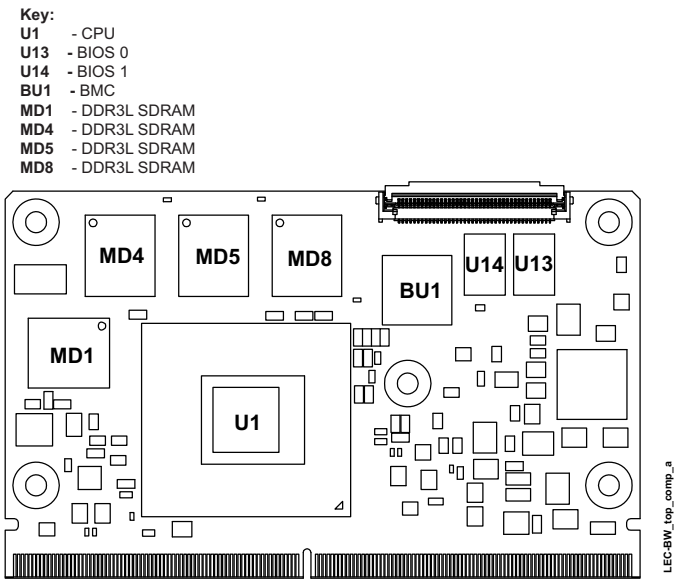


Figure 2-1: Component Locations (Top Side)

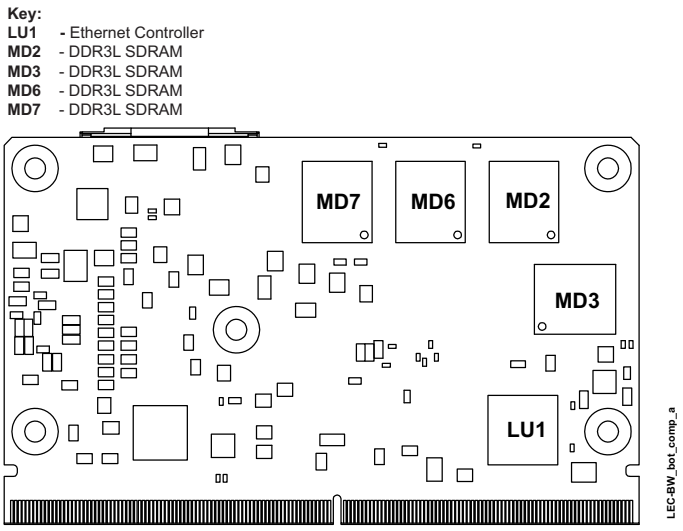


Figure 2-2: Component Locations (Bottom Side)

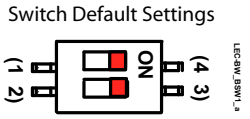
2.2 Connectors, Switches, and LEDs

Table 2-2 describes the connectors, switches, and LEDs shown in Figure 2-3 and Figure 2-4.

Table 2-2: Module Connector Description

Connector#	Board Access	Description
CN1	Top	40-pin, DB40 Front-Flip connector for debug card (Molex, 502790-4091)
GF1 - SMARC Primary and Secondary (P and S)	Top/ Bottom	314-pin, MXM edge connector for Memory, Video, and I/O functions
LED1	Top	Blue LED indicating system status activities for HW Reset, SW Reset, Power Up, Power Down, Reset Button, and Power Button

Table 2-2: Module Connector Description (Continued)

LED2	Top	Green LED for Power On in S0 state, controlled by SLP_S3#
LED3	Top	Red LED for Watchdog time out, driven by SEMA and cleared by software or reset button
SW1	Top	4-pin dip switch for • Setting BIOS Boot (1=Boot from SPI1, 4=Boot from SPI0 [default]) • Selecting BIOS Mode (2=Failsafe BIOS, 3=Normal BIOS [default]) 

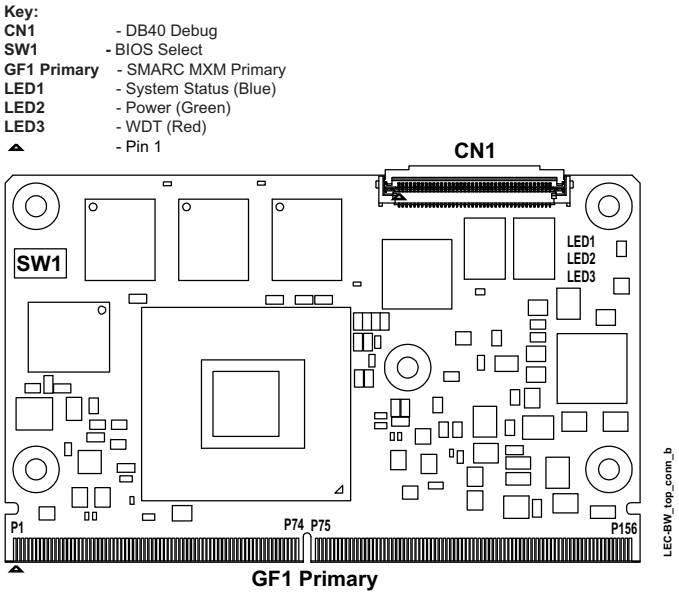


Figure 2-3: Connector Locations (Top Side)

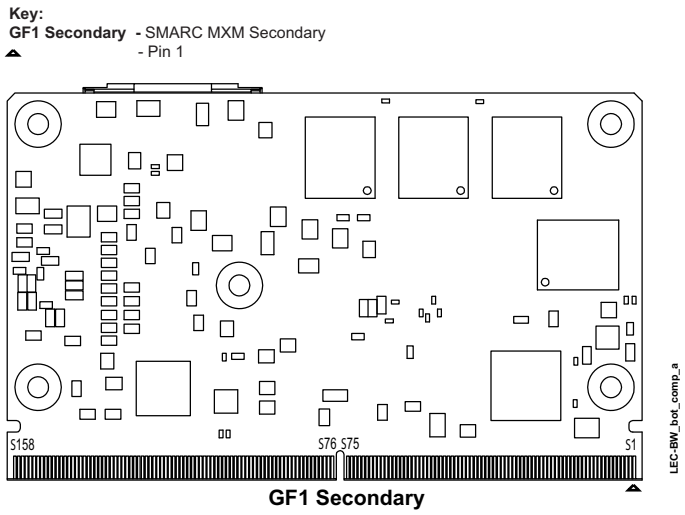


Figure 2-4: Connector Locations (Bottom Side)

2.3 Component Features

This section further describes the supported features of the LEC-BW major, on-board hardware components.

2.3.1 CPU

The LEC-BW product family offers the following versions of the Intel Pentium and Celeron N-Series CPU, System-on-Chip (SoC): the N3710 Pentium (Quad Core with Gfx 700MHz), the N3160 Celeron (Quad Core with Gfx 640MHz), the N3060 Celeron (Dual Core with Gfx 600MHz), and the N3010 Celeron (Dual Core with Gfx 600MHz). The LEC-BW product family also includes a lower-cost alternative: the x5-E8000 Atom with Gfx 320MHz. N-Series CPUs feature the Intel Architecture and are manufactured based on Intel's 14-nanometer technology. Refer to the N-series SoC data sheet on the Intel web site. Other CPU SKUs are available on request.

2.3.2 SDRAM

The LEC-BW employs one channel of 64-bit DDR3L on-board memory. Eight SDRAM memory chips provide up to 32Gb of low-voltage non-ECC, unbuffered system memory. Refer to the MT41K SDRAM data sheet on the Micron web site.

Depending on the DRAM chips featured on the module, the following total DRAM capacities are supported:

- 8x 126M8 = 1 GB
- 8x 256M8 = 2 GB
- 8x 512M8 = 4 GB
- 8x 1M8 = 8 GB

2.3.3 I211 LAN Controller

The Intel I211 provides a single-port controller that supports GbE functionality using the high-speed PCIe standard, v2.1 (2.5GT/s). The I211 features an integrated PHY, which enables 1000BASE-T implementations such as rack-mounted or pedestal servers in add-on NIC or LAN-on-Motherboard (LOM) designs. Other implementations include blade servers such as LOMs or mezzanine cards as well as embedded applications such as switch add-on cards and network appliances. Refer to the Intel I211 Ethernet Controller data sheet on the Intel web site.

2.3.4 PTN3460i eDP-to-LVDS Converter

The PTN 3460i supports single-bus or dual-bus LVDS signalling with color depths of 18 bits per pixel or 24 bits per pixel and pixel clock frequency up to 112MHz. The LVDS data packing can be done either in VESA or JEIDA formats. Also, the DP AUX interface transports I2C-over-AUX commands and support EDID-DDC communication with LVDS panel. To support panels without EDID ROM, the PTN3460 can emulate EDID ROM behavior, avoiding specific changes in system video BIOS. Find more details on the NXP website.

2.3.5 PCA9535A GPIO Expander

The PCA9535A is a 24-pin device that provides 16 bits of General Purpose parallel Input/Output (GPIO) expansion for I2C-bus/SMBUS applications. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion register. The operating power supply voltage range of the PCA535A is 1.65V to 5.5V. Find more details on the NXP website.

2.3.6 SMBus Slave Addresses

Table 2-3 lists the corresponding slave addresses of the devices on the SMBus.

Table 2-3: SMBus Slave Addresses

Address (HEX)	Function	Device
(40)	GPIO	PCA9535A
(50)	BMC/SEMA	BMC
(C0)	eDP to LVDS	PTN3460i
(A0)	DDR3L channel A	DDR3L memory
(92)	Thermal Sensor	LM73

3 Interfaces

This section provides descriptions of the interfaces and signals within the SMARC P-S (Primary-Secondary) connector. Refer to the SMARC specification at: http://www.sget.org/standards/qseven.html for definitions of the SMARC interfaces. The SMARC P-S (Primary-Secondary) connector provides the following interfaces:

- Video
- Camera
- HD Audio
- PCI Express (PCIe)
- Gb Ethernet
- USB 2.0
- USB 3.0
- SATA
- I2C
- SPI
- Serial UART
- I2S (Audio)
- SD/SDIO
- eMMC
- GPIO
- Debug

ADLINK Technology, Inc. only supports the features/ options tested and listed in this manual. The main chips used in the LEC-BW may provide more features or options than are listed for the LEC-BW, but some of these features or options are not supported on the module and will not function as specified in the chip documentation.

3.1 Display Interfaces

The LEC-BW supports three independent display interfaces. This section describes all three interfaces including the standard and optional configurations for each.

3.1.1 18/24-Bit LVDS LCD (Primary Display)

The LVDS interface is connected to the DDI1 port of the CPU, and the translation is made by the eDP-to-LVDS converter. The standard LEC-BW configuration supports a single channel LVDS interface with a max. resolution of 1280x720 pixels at 60Hz, as defined by the SMARC specification. As a custom option, a second LVDS channel can be supported (separate order number for both, module and carrier.) The dual channel LVDS interface supports resolutions up to 1920x1200 at 60Hz. Refer to the NXP PTN3460I, eDP-to-LVDS converter datasheet. See the LEC-BW display interface diagrams in Section 3.1.3.

3.1.2 HDMI (Secondary Display)

The second digital display is an HDMI interface, which originates from the DDI2 port of the CPU. The standard LEC-BW display configuration supports HDMI (TMDS) output to the display. The standard HDMI interface provides the following features:

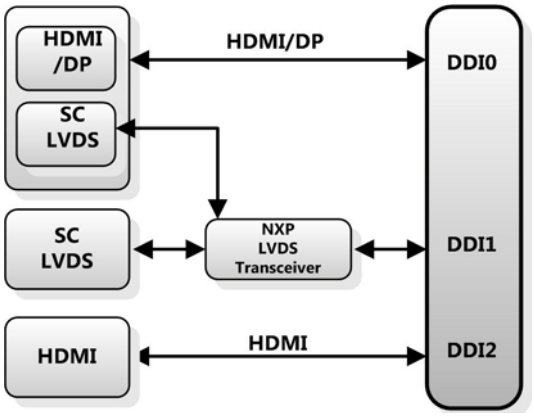
- 1 clock pair
- 3 Data pairs
- Service signals
- HDMI resolutions up to 3840x2160 @ 30Hz or 2560x1600 @ 60Hz

3.1.3 HDMI/Display Port (DP) [Third Display]

An optional configuration (separate order number for both, module and carrier) supports a third digital display, which can be either HDMI (TMDS) or Display Port output. It originates from DDI0. This implementation re-uses the SMARC parallel LCD pins, which would otherwise go unused on the LEC-BW. The optional custom display configuration provides the following features:

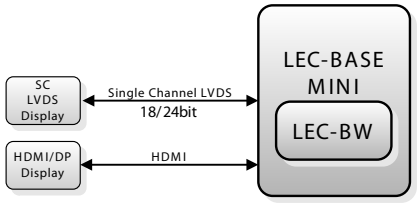
- 1 clock pair
- 3 Data pairs
- Service signals
- HDMI or DP resolutions up to 3840x2160 @ 30Hz or 2560x1600 @ 60Hz
- Compliant with the HDMI 1.4b specification.
- Compliant with the DP 1.1a specification.

The following diagram represents the standard and optional display interface configurations supported by the LEC-BW when mounted on the LEC-BASE MINI carrier.

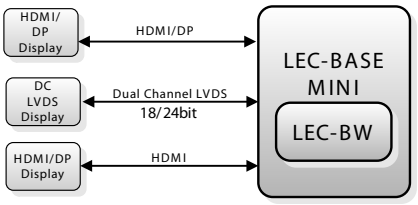


The following diagram represents an overview of the standard and optional display interface configurations supported by the LEC-BW when mounted on both versions of the LEC-BASE MINI carrier. The LEC-BASE MINI (Standard) supports the standard dual display configuration, while LEC-BASE MINI (Custom) supports the custom configuration with a third display and a second LVDS channel.

LEC-BW (Standard)



LEC-BW (Custom Option)



3.2 Camera MIPI-CSI

The LEC-BW brings out signals for two MIPI-CSI 2.0 (serial) camera interfaces, one with two data lanes and one with four data lanes, supporting up to 800 Mbit/s of actual pixels. The following bullets highlight the imaging capabilities of the Camera interface.

- Sensor interface for 2 sensors: x4, x2
- Up to 2 simultaneous sensors
- 5MP 2-D image capture
- Up to 1080p30 2-D video capture
- RAW 8, 10, 12, 14, RGB444, 565, 888, YUV420, 422, JPEG input formats
- YUV422, YUV420, RAW output formats
- Special features
  - Image and video stabilization
  - Low light noise reduction
  - Burst mode capture
  - Memory to memory processing
  - 3A (Auto Exposure [AE], Auto White Balance [AWB], and Auto Focus [AF])
  - High Dynamic Range (HDR)
  - Multi focus
  - Zero shutter lag

3.3 Audio (HDA)

The CPU provides an HDA controller, which communicates over the Intel HDA serial link with internal CODECs on the CPU or external CODECs on the baseboard. HDA signals are brought out through the I2S2 pins on the SMARC connector and are multiplexed with LPE_I2S audio signals. When HDA is active, LPE audio is disabled. The following list highlights the features of the audio interface.

- Decode: MP3, AAC-LC, HE-ACC v1/2, WMA9, 10, PRO, Lossless, Voice, MPEG layer 2, Real Audio, OggVorbis, FLAC, DD/DD+
- Encode: MP3, ACC-LC, WMA, DD-2channel
- Supports MSI and legacy interrupt delivery
- Support for ACPI D3 and D0 Device States
- Supports up to:
  - 6 streams (three input, three output)
  - 16 channels per stream
  - 32 bits/sample
  - 192KHz sample rate
- 24 MHz HDA_CLK supports:
  - SDO double pumped at 48Mb/s
  - SDI single pumped at 24Mb/s
- Supports 1.5V and 1.8V modes
- Supports optional Immediate Command/Response mechanism

A camera driver is required for each OS.

3.4 PCI Express (PCIe)

The CPU features four PCIe x1 ports, and the LEC-BW module uses three of them for the PCIe interface and one of them for the Gigabit Ethernet interface. The PCIe interface supports the PCIe Base Specification 2.0 with a maximum signal rate of 5 GT/s and can be configured to support PCIe edge cards or Express Cards.

3.5 Gigabit Ethernet

The on-board Intel I211IT Ethernet controller uses PCIe x1 (v2.1) bus signals from the CPU to enable 10T/100TX/1000T operation through integrated MAC, PHY, and MDI interfaces.

3.6 USB Ports

The USB interface originates from two host controllers on the CPU that provide four USB 2.0 host ports and one USB 3.0 host port.

3.6.1 USB 2.0

Three of the four USB 2.0 ports use the USB 0-2 pins on the SMARC connector (0 = host; 1 = host; 2 = host.) The fourth USB 2.0 port uses the AFB_DIFF2 pins (S68-S69) on the SMARC connector.

3.6.2 USB 3.0

The USB 3.0 port uses the AFB_DIFF pins on the SMARC connector and map to the AFB header on the LEC-BASE baseboard. See pins S62/S63 and S65/S66 in Table 3-2.

3.7 SATA

The SATA interface provides two GEN3 ports. The SATA0 pins on the SMARC connector provide one port. The AFB-DIFF 3 and 4 pins provide the second port. The interface supports up to 6Gb/s for each port.

3.8 I2C Bus

The LEC-BW provides five interfaces through the I2C bus for general purpose signals with operating speeds up to 400kHz. The following table maps the I2C interfaces to their corresponding pins on the SMARC interface connector.

SMARC Pins	I2C Interfaces
P105/P106	HDMI Control
P121/P122	PM
S5/S7	Camera
S48/S49	GP
S139/S140	LCD/EDID

3.9 SPI

The CPU implements two SPI controllers. One SPI controller connects to two SPI flash devices on the module and to the DB40 connecter. The second SPI controller supports devices on the carrier through the SMARC (MXM3) connector pins (SPI0 and SPI1).

3.10 Serial (UART)

The LEC-BW provides two serial interfaces: one high-speed, 4-wire port with TX/RX and RTS#/CTS# signals and one 2-wire port (with TX/RX only.)

3.11 SD/SDIO Interface

Four parallel data lines comprise the SD/SDIO interface, supporting SD Card sockets.

3.12 eMMC Interface

The LEC-BW provides one 8-bit eMMC interface port, brought out from the CPU through the SDMMC pins on the SMARC connector.

3.13 GPIO

The LEC-BW provides 12 GPIO signals from the CMOS device on the module. The GPIO signals can be utilized for General Purpose IO interfaces as well as HDA reset. Table 3-1 provides the default functions of the GPIO signals.

Table 3-1: GPIO Default Settings

SMARC Connector Pin	Default Function
GPIO0	GPIO
GPIO1	GPIO
GPIO2	GPIO
GPIO3	GPIO
GPIO4	HDA_RST#
GPIO5	GPIO
GPIO6	GPIO
GPIO7	GPIO
GPIO8	GPIO
GPIO9	GPIO
GPIO10	GPIO
GPIO11	GPIO

The signals GPIO0-GPIO3 alternatively can be used for MIPI CSI camera signals, CAM0_PWR#, CAM1_PWR#, CAM0_RST#, CAM1_RST#. This requires a separate module order number (BOM option). Its usage depends on the availability of camera drivers of the installed operating system. A camera add-on card is needed for the LEC_BASE MINI carrier.

3.14 LPC Debug Interface

A 40-pin, front flip, DB40 connector allows access to the system to debug and update the BIOS, BMC, and OS code. (Refer to “Debug (DB40) Connector Signals” on page 31.)

3.15 SMARC Interface Signals

Table 3-2 provides the supported pin signal definitions for the SMARC connector. Refer to the SMARC specification at http://www.sget.org/standards/smarc.html for further details of the SMARC signals.

Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
		S1	Not connected
P1	Not connected	S2	Not connected
P2	GND	S3	GND
P3	CSI1_CK+ (CSI1 differential clock inputs.)	S4	Not connected
P4	CSI1_CK- (CSI1 differential clock inputs.)	S5	I2C_CAM_CK (Serial / Parallel camera support link - I2C clock)
P5	Not connected	S6	CAM_MCK (Master clock output for CSI camera support (may be used for CSI0 and / or CSI1)
P6	Not connected	S7	I2C_CAM_DAT (Serial / Parallel camera support link - I2C data)
P7	CSI1_D0+ (CSI1 differential data inputs.)	S8	CSI0_CK+ (CSI0 differential clock inputs.)
P8	CSI1_D0- (CSI1 differential data inputs.)	S9	CSI0_CK- (CSI0 differential clock inputs.)
P9	GND	S10	GND
P10	CSI1_D1+ (CSI1 differential data inputs.)	S11	CSI0_D0+ (CSI0 differential data inputs.)
P11	CSI1_D1- (CSI1 differential data inputs.)	S12	CSI0_D0- (CSI0 differential data inputs.)
P12	GND	S13	GND
P13	CSI1_D2+ (CSI1 differential data inputs.)	S14	CSI0_D1+ (CSI0 differential data inputs)
P14	CSI1_D2- (CSI1 differential data inputs.)	S15	CSI0_D1- (CSI0 differential data inputs)
P15	GND	S16	GND
P16	CSI1_D3+ (CSI1 differential data inputs.)	S17	AFB0_OUT (General purpose AFB output; maps to PMU_SLP_S3# on the SOC)
P17	CSI1_D3- (CSI1 differential data inputs.)	S18	AFB1_OUT (General purpose AFB output; maps to PMU_SLP_S4# on the SOC)
P18	GND	S19	AFB2_OUT (General purpose AFB output; maps to PMU_SUS_STAT# on the SOC)
P19	GBE_MDI3- (Bi-directional transmit/ receive pair 3 to magnetics [Media Dependent Interface])	S20	Not connected
P20	GBE_MDI3+(Bi-directional transmit/ receive pair 3 to magnetics [Media Dependent Interface])	S21	Not connected
P21	GBE_LINK100# (Link Speed Indication LED for 100Mbps; able to sink 24mA or more carrier LED current)	S22	Not connected
P22	GBE_LINK1000# (Link Speed Indication LED for 1000Mbps; able to sink 24mA or more carrier LED current)	S23	AFB6_PTIO (EN_OC# for USB SS)
P23	GBE_MDI2- (Bi-directional transmit/ receive pair 2 to magnetics [Media Dependent Interface])	S24	AFB7_PTIO (PCU_SMB_ALERT#)

Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P24	GBE_MDI2+ (Bi-directional transmit/ receive pair 2 to magnetics [Media Dependent Interface])	S25	GND
P25	GBE_LINK_ACT# (Link / Activity Indication LED Driven low on Link [10, 100 or 1000 mbps] Blinks on Activity; able to sink 24mA or more Carrier LED current)	S26	SDMMC_D0 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P26	GBE_MDI1- (Bi-directional transmit/ receive pair 1 to magnetics [Media Dependent Interface])	S27	SDMMC_D1 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P27	GBE_MDI1+ (Bi-directional transmit/ receive pair 1 to magnetics [Media Dependent Interface])	S28	SDMMC_D2 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P28	GBE_CTREF (Center-Tap reference voltage for GBE0 Carrier board Ethernet magnetic [if required by the Module GBE PHY])	S29	SDMMC_D3 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P29	GBE0_MDI0- (Bi-directional transmit/ receive pair 0 to magnetics [Media Dependent Interface])	S30	SDMMC_D4 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P30	GBE0_MDI0+ (Bi-directional transmit/ receive pair 0 to magnetics [Media Dependent Interface])	S31	SDMMC_D5 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P31	SPI0_CS1# (SPI0 Master Chip Select 1 output)	S32	SDMMC_D6 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P32	GND	S33	SDMMC_D7 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P33	SDIO_WP (SDIO card Write Protect; 1K pull-up to 3.3V)	S34	GND
P34	SDIO_CMD (SDIO card Command line)	S35	SDMMC_CK (clock)
P35	SDIO_CD# (SDIO Card Detect; 1K pull-up to 3.3V)	S36	SDMMC_CMD (command line)
P36	SDIO_CK (SDIO card Clock)	S37	SDMMC_RST# (Reset signal to eMMC device)
P37	SDIO_PWR_EN (SDIO card Power Enable)	S38	Not connected
P38	GND	S39	Not connected
P39	SDIO_D0 (SDIO card 4-bit data path)	S40	Not connected
P40	SDIO_D1 (SDIO card 4-bit data path)	S41	Not connected
P41	SDIO_D2 (SDIO card 4-bit data path)	S42	Not connected
P42	SDIO_D3 (SDIO card 4-bit data path)	S43	Not connected
P43	SPI0_CS0# (SPI0 Master Chip Select 0 output; use to select carrier SPI boot device)	S44	Not connected
P44	SPI0_CK (SPI0 Master Clock output)	S45	Not connected
P45	SPI0_DIN (SPI0 Master Data input [input to CPU, output from SPI device])	S46	Not connected
P46	SPI0_DO (SPI0 Master Data output [output from CPU, input to SPI device])	S47	GND

Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P47	GND	S48	I2C_GP_CK (I2C General Purpose clock signal)
P48	SATA0_TX+ (Differential SATA 0 transmit data Pair; 0.1 uF 0402 capacitor on module)	S49	I2C_GP_DAT I2C (General Purpose data signal)
P49	SATA0_TX- (Differential SATA 0 transmit data Pair; 0.1 uF 0402 capacitor on module)	S50	HDA_SYNC (Intel HD Audio Sync: 48KHz fixed rate)
P50	GND	S51	HDA_SDO (Intel HD Audio Data Out: Serial TMD data output to the codec(s). The serial output is double-pumped for a bit rate of 48Mb/s.)
P51	SATA0_RX+ (Differential SATA 0 receive data Pair; 0.1 uF 0402 capacitor on module)	S52	HDA_SDI0 (Intel HD Audio Data In: Serial TMD data input from the codec(s). The serial input is single-pumped for a bit rate of 24Mb/s)
P52	SATA0_RX- (Differential SATA 0 receive data Pair; 0.1 uF 0402 capacitor on module)	S53	HDA_CLK (Intel Audio Bit Clock [output]: 24MHz serial data clock generated by the Intel HD Audio controller.
P53	GND	S54	SATA_ACT# (Active low SATA activity indicator If implemented, able to sink 24mA or more Carrier LED current)
P54	SPI1_CS0# (SPI1 Master Chip Select 0 output)	S55	Not connected
P55	SPI1_CS1# (SPI1 Master Chip Select 1 output)	S56	Not connected
P56	SPI1_CK (SPI1 Master Clock output)	S57	Not connected
P57	SPI1_DIN (SPI1 Master Data input [input to CPU, output from SPI device])	S58	Not connected
P58	SPI1_DO (SPI1 Master Data output [output from CPU, input to SPI device])	S59	Not connected
P59	GND	S60	Not connected
P60	USB0+ (Differential USB0 data pair)	S61	GND
P61	USB0- (Differential USB0 data pair)	S62	AFB_DIFF0+ (maps to USB3_TX_P [USB 3.0] on the SOC)
P62	USB0_EN_OC# (Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up is present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 of *SMARC Specification.*)	S63	AFB_DIFF0- (maps to USB3_TX_N [USB 3.0] on the SOC)
P63	Not connected	S64	GND
P64	USB0_OTG_ID (USB OTG ID input, active high)	S65	AFB_DIFF1+ (maps to USB3_RX_P [USB 3.0] on the SOC)
P65	USB1+ (Differential USB1 data pair)	S66	AFB_DIFF1- (maps to USB3_RX_N [USB 3.0] on the SOC)
P66	USB1- (Differential USB1 data pair)	S67	GND

Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P67	USB1_EN_OC# (Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up is present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 of *SMARC Specification.*)	S68	AFB_DIFF2+ (maps to USB_D3_P [USB 2.0] on the SOC)
P68	GND	S69	AFB_DIFF2- (maps to USB_D3_N [USB 2.0] on the SOC
P69	USB2+ (Differential USB2 data pair)	S70	GND
P70	USB2- (Differential USB2 data pair)	S71	AFB_DIFF3+ (maps to SATA_TX1_P on the SOC)
P71	USB2_EN_OC# (Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up ***shall*** be present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 of *SMARC Specification*.)	S72	AFB_DIFF3- (maps to SATA_TX1_N on the SOC)
P72	PCIE_C_PRSNT# (PCIe Port C present input. Pulled up or terminated on Module)	S73	GND
P73	PCIE_B_PRSNT# (PCIe Port B present input. Pulled up or terminated on Module)	S74	AFB_DIFF4+ (maps to SATA_RX1_P on the SOC)
P74	PCIE_A_PRSNT# (PCIe Port A present input. Pulled up or terminated on Module)	S75	AFB_DIFF4- (maps to SATA_RX1_N on the SOC)
P75	PCIE_A_RST# (PCIe Port A reset output)	S76	PCIE_B_RST# (PCIe Port B reset output, active low)
P76	PCIE_C_CKREQ# (PCIe Port C clock request input. Pulled up or terminated on Module)	S77	PCIE_C_RST# (PCIe Port A reset output, active low)
P77	PCIE_B_CKREQ# (PCIe Port B clock request input. Pulled up or terminated on Module)	S78	PCIE_C_RX+ (Differential PCIe Link C receive data pair 0. No coupling caps on Module)
P78	PCIE_A_CKREQ# (PCIe Port A clock request input. Pulled up or terminated on Module)	S79	PCIE_C_RX- (Differential PCIe Link C receive data pair 0. No coupling caps on Module)
P79	GND	S80	GND
P80	PCIE_C_REFCK+ (Differential PCIe Link C reference clock output. DC coupled)	S81	PCIE_C_TX+ (Differential PCIe Link C transmit data pair 0. Series coupling caps are on the Module. Caps are 0201 package 0.1uF)
P81	PCIE_C_REFCK- (Differential PCIe Link C reference clock output. DC coupled)	S82	PCIE_C_TX- (Differential PCIe Link C transmit data pair 0. Series coupling caps are on the Module. Caps are 0201 package 0.1uF)
P82	GND	S83	GND
P83	PCIE_A_REFCK+ (Differential PCIe Link A reference clock output. DC coupled)	S84	PCIE_B_REFCK+ (Differential PCIe Link B reference clock output; DC coupled)
P84	PCIE_A_REFCK- (Differential PCIe Link A reference clock output. DC coupled)	S85	PCIE_B_REFCK- (Differential PCIe Link B reference clock output; DC coupled)

Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P85	GND	S86	GND
P86	PCIE_A_RX+ (Differential PCIe Link A receive data pair 0. No coupling caps on Module)	S87	PCIE_B_RX+ (Differential PCIe Link B receive data pair 0. No coupling caps on Module)
P87	PCIE_A_RX- (Differential PCIe Link A receive data pair 0. No coupling caps on Module)	S88	PCIE_B_RX- (Differential PCIe Link B receive data pair 0. No coupling caps on Module)
P88	GND	S89	GND
P89	PCIE_A_TX+ (Differential PCIe Link A transmit data pair 0. Series coupling capacitors are on the Module. 0.1 uF 0201 capacitor are on module)	S90	PCIE_B_TX+ (Differential PCIe Link B transmit data pair 0. Series coupling caps are on the Module Caps are 0201 package 0.1uF)
P90	PCIE_A_TX- (Differential PCIe Link A transmit data pair 0. Series coupling capacitors are on the Module. 0.1 uF 0201 capacitor are on module)	S91	PCIE_B_TX- (Differential PCIe Link B transmit data pair 0. Series coupling caps are on the Module Caps are 0201 package 0.1uF)
P91	GND	S92	GND
P92	HDMI_D2+ (TMDS / HDMI data 2 differential pair)	S93	DP_D0+ / HDMI_B_D2+ (Display Port or HDMI data pair 0; output)
P93	HDMI_D2- (TMDS / HDMI data 2 differential pair)	S94	DP_D0- / HDMI_B_D2- (Display Port or HDMI data pair 0; output)
P94	GND	S95	GND
P95	HDMI_D1+ (TMDS / HDMI data 1 differential pair)	S96	DP_D1+ / HDMI_B_D1+ (Display Port or HDMI data pair 1; output)
P96	HDMI_D1- (TMDS / HDMI data 1 differential pair)	S97	DP_D1- / HDMI_B_D1- (Display Port or HDMI data pair 1; output)
P97	GND	S98	GND)
P98	HDMI_D0+ (TMDS / HDMI data 0 differential pair)	S99	DP_D2+ / HDMI_B_D0+ (Display Port or HDMI data pair 2; output)
P99	HDMI_D0- (TMDS / HDMI data 0 differential pair)	S100	DP_D2- / HDMI_B_D0- (Display Port or HDMI data pair 2; output)
P100	GND	S101	GND
P101	HDMI_CK+ (TMDS / HDMI clock output differential pair)	S102	DP_D3+ / HDMI_B_CK+ (Display Port data pair or HDMI clock pair; output)
P102	HDMI_CK- (TMDS / HDMI clock output differential pair)	S103	DP_D3- / HDMI_B_CK- (Display Port data pair or HDMI clock pair; output)
P103	GND	S104	GND
P104	HDMI_HPD (HDMI Hot Plug Detect input)	S105	DP_HDP / HDMI_B_HDP (Display Port or HDMI Hot Plug Detect; input)
P105	HDMI_CTRL_CK (I2C clock line dedicated to HDMI)	S106	DP_AUX+ / HDMI_B_CTRL_CK (Display Port Auxiliary Channel pair or HDMI control clock; input/output)
P106	HDMI_CTRL_DAT (I2C data line dedicated to HDMI)	S107	DP_AUX- / HDMI_B_CTRL_DAT (Display Port Auxiliary Channel pair or HDMI control data; input/output)
P107	Not Connected	S108	AUX_SEL / HDMI_B_CEC (DP or HDMI Select or HDMI Consumer Electronic Control, 1-wire peripheral control interface)
P108	GPIO0 (General Purpose IO [Output recommended])	S109	Not connected
P109	GPIO1 (General Purpose IO [Output recommended])	S110	GND

Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P110	GPIO2 (General Purpose IO [Output recommended])	S111	LVDS_B_0+ (LVDS control channel data pair; output)
P111	GPIO3 (General Purpose IO [Output recommended])	S112	LVDS_B_0- (LVDS control channel data pair; output)
P112	HDA_RST# (HDA reset output)	S113	Not connected
P113	GPIO5 (General Purpose IO [Output recommended])	S114	LVDS_B_1+ (LVDS control channel data pair; output)
P114	GPIO6 (General Purpose IO [Input recommended])	S115	LVDS_B_1- (LVDS control channel data pair; output)
P115	GPIO7 (General Purpose IO [Input recommended])	S116	Not connected
P116	GPIO8 (General Purpose IO [Input recommended])	S117	LVDS_B_2+ (LVDS control channel data pair; output)
P117	GPIO9 (General Purpose IO [Input recommended])	S118	LVDS_B_2- (LVDS control channel data pair; output)
P118	GPIO10 (General Purpose IO [Input recommended])	S119	GND
P119	GPIO11 (General Purpose IO [Input recommended])	S120	LVDS_B_CK+ (LVDS control channel clock pair; output)
P120	GND	S121	LVDS_B_CK- (LVDS control channel clock pair; output)
P121	I2C_PM_CK (Power management I2C bus clock)	S122	LVDS_B_3+ (LVDS control channel data pair; output)
P122	I2C_PM_DAT(Power management I2C bus data)	S123	LVDS_B_3+ (LVDS control channel data pair; output)
P123	BOOT_SEL0# (Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.)	S124	GND
P124	BOOT_SEL1# (Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.)	S125	LVDS_A_0+ (LVDS control channel data pair; output)
P125	BOOT_SEL2# (Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.)	S126	LVDS_A_0- (LVDS control channel data pair; output)
P126	RESET_OUT# (General purpose reset output to Carrier board.)	S127	LVDS_BKLT_EN (High enables panel backlight)
P127	RESET_IN# (Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise. Pulled up on Module. Driven by OD part on Carrier.)	S128	LVDS_A_1+ (LVDS control channel data pair; output)
P128	POWER_BTN# (Power-button input from Carrier board. Carrier to float the line in inactive state. Active low, level sensitive. De-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.)	S129	LVDS_A_1- (LVDS control channel data pair; output)
P129	SER0_TX (Asynchronous serial port data out)	S130	GND
P130	SER0_RX (Asynchronous serial port data in)	S131	LVDS_A_2+ (LVDS control channel data pair; output)
P131	SER0_RTS# (Request to Send handshake line for SER0)	S132	LVDS_A_2- (LVDS control channel data pair; output)

Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P132	SER0_CTS# (Clear to Send handshake line for SER0)	S133	LCD_VDD_EN (High enables panel VDD)
P133	GND	S134	LVDS_A_CK+ (LVDS control channel clock pair; output)
P134	SER1_TX (Asynchronous serial port data out)	S135	LVDS_A_CK- (LVDS control channel clock pair; output)
P135	SER1_RX (Asynchronous serial port data in)	S136	GND
P136	Not connected	S137	LVDS_A_3+ (LVDS control channel clock pair; output)
P137	Not connected	S138	LVDS_A_3- (LVDS control channel clock pair; output)
P138	Not connected	S139	LVDS_DDC_CLK (I2C clock – to read LCD display EDID EEPROMs)
P139	Not connected	S140	LVDS_DDC_DAT (I2C data – to read LCD display EDID EEPROMs)
P140	Not connected	S141	LCD_BKLT_PWM (Display backlight PWM control)
P141	Not connected	S142	Not connected
P142	GND	S143	GND
P143	Not connected	S144	EDP_HPD (eDP Hot Plug Detect pin)
P144	Not connected	S145	WDT_TIME_OUT# (Watchdog Timer Output)
P145	Not connected	S146	PCIE_WAKE (PCIe wake up interrupt to host – common to PCIe; links A, B, C – pulled up or terminated on Module)
P146	Not connected	S147	VDD_RTC (Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap. See ***Section 7.3 RTC Voltage Rail*** of the SMARC specification for an important safety note on the implementation of lithium backup batteries.)
P147	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S148	LID# (Lid open/close indication to Module. Low indicates lid closure, which system ***may*** use to initiate a sleep state. Carrier to float the line in inactive state. Active low, level sensitive. De-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.)
P148	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S149	SLEEP# (Sleep indicator from Carrier board; sourced from user Sleep button or Carrier logic. Carrier to float the line in inactive state. Active low, level sensitive; de-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier.)

Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P149	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S150	VIN_PWR_BAD# (Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) ***is not*** enabled while this signal is held low by the Carrier. Pulled up on Module. Driven by OD part on Carrier.)
P150	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S151	CHARGING# (Held low by Carrier during battery charging. Carrier to float the line when charge is complete. Pulled up on Module. Driven by OD part on Carrier.)
P151	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S152	CHARGER_PRSNT# (Held low by Carrier if DC input for battery charger is present. Pulled up on Module. Driven by OD part on Carrier.)
P152	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S153	CARRIER_STBY# (The Module drives this signal low when the system is in a standby power state)
P153	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S154	CARRIER_PWR_ON (Carrier board circuits [apart from power management and power path circuits] ***are*** powered up until the Module asserts the CARRIER_PWR_ON signal)
P154	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S155	FORCE_RECOV# (Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery function, then a low on the Module FORCE_RECOV# pin ***may*** invoke the SOC native Force Recovery mode – such as over a Serial Port. Pulled up on Module. Driven by OD part on Carrier.)
P155	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S156	BATLOW# (Battery low indication to Module. Carrier to float the line in inactive state. Pulled up on Module. Driven by OD part on Carrier.)
P156	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S157	TEST# (Held low by Carrier to invoke Module vendor specific test function(s). Pulled up on Module. Driven by OD part on Carrier.)
		S158	GND

NOTE: The # symbol indicates the signal is Active Low.

3.16 Debug (DB40) Connector Signals

Table 3-3 lists the pin signals of the CN1 connector, which provides 40 pins, 1 row, consecutive sequence with 0.02" (0.50mm) pitch.

Table 3-3: Debug Interface Signals (CN1)

Pin #	Interface	Signal
1	**NC**	RESVD
2	**SMC Debug**	SMC_STATUS
3		BIOS_MODE
4		SEL_BIOS
5		POSTWDT_DIS#
6	**Test Point**	SUS_S5#
7		SUS_S4#
8		SUS_S3#
9		CB_PWROK
10		CB_RESET#
11		SYS_RESET#
12		PWRBTN#
13	**SMC Program Interface**	SMC_OCD0B
14		SMC_OCD0A
15		SMC_CLK
16		SMC_DATA
17		SMC_RESET_IN#
18		SMC_FLMD0
19		SMC_RXD6
20		SMC_TXD6
21		GND3
22		3V3_DUAL
23		3V3_SMC1
24	**LPC Debug Card Interface**	LPC_AD0
25		LPC_AD1
26		LPC_AD2
27		LPC_AD3
28		LPC_FRAME#
29		CLK33_LPC
30		RST#
31		BIOS_DIS0
32		GND2
33		LPC_3V3
34	**SPI Program Interface**	SPI_BIOS_CLK
35		SPI_BIOS_MOSI
36		SPI_BIOS_MISO
37		SPI_BIOS_CS1#
38		SPI_BIOS_CS0#
39		GND1
40		VCC_SPI_IN

NOTE: The gray table cells denote ground. The # symbol indicates the signal is Active Low.

4 Utilities

This chapter provides information on how to read information from and configure the BIOS Setup utility, the SEMA utility, the Watchdog Timer utility, and the board temperature sensors on the LEC-BW.

4.1 BIOS

The LEC-BW features an AMI BIOS. The default settings provide a “ready to run” system, even without a BIOS setup backup battery.

The BIOS is located in flash memory and can be easily updated with software under DOS.

All setup changes of the BIOS are stored in the CMOS RAM.

The battery on the baseboard will provide power to store that information for over two years without board activation.

This section presents the five primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right hand column of the respective table.

Table 4-1: BIOS Setup Menu Structure

Main	Advanced	Security	Boot	Save & Exit
• System Information • Processor Information • VGA Firmware Version • Memory Information • SOC Information • System Management ► • System Date • System Time	• CPU► • Graphics► • Memory► • SATA► • USB► • Network ► • PCIe ► • Configuration • ACPI and Power Management► • Sound► • Serial Port Console► • Thermal► • Miscellaneous►	• Password Description► • Secure Boot Menu►	• Boot Configuration • CSM Configuration ►	• Reset Options ► • Save Options ►

Notes:
► indicates a submenu
Gray text indicates info only

4.1.1 Starting the BIOS Setup Utility

Use the following bullets to initiate start-up activity for the BIOS Setup Utility.

- ► Press <DEL> during power up to start the BIOS setup utility.
- ► Press <F11> during power up to start the Boot menu.
- ► Press <END> during power up to return BIOS settings to default.

4.1.2 Main Menu

The Main Menu provides read-only information about your system and also allows you to set the System Date and Time. Refer to the tables below for details of the submenus and settings.

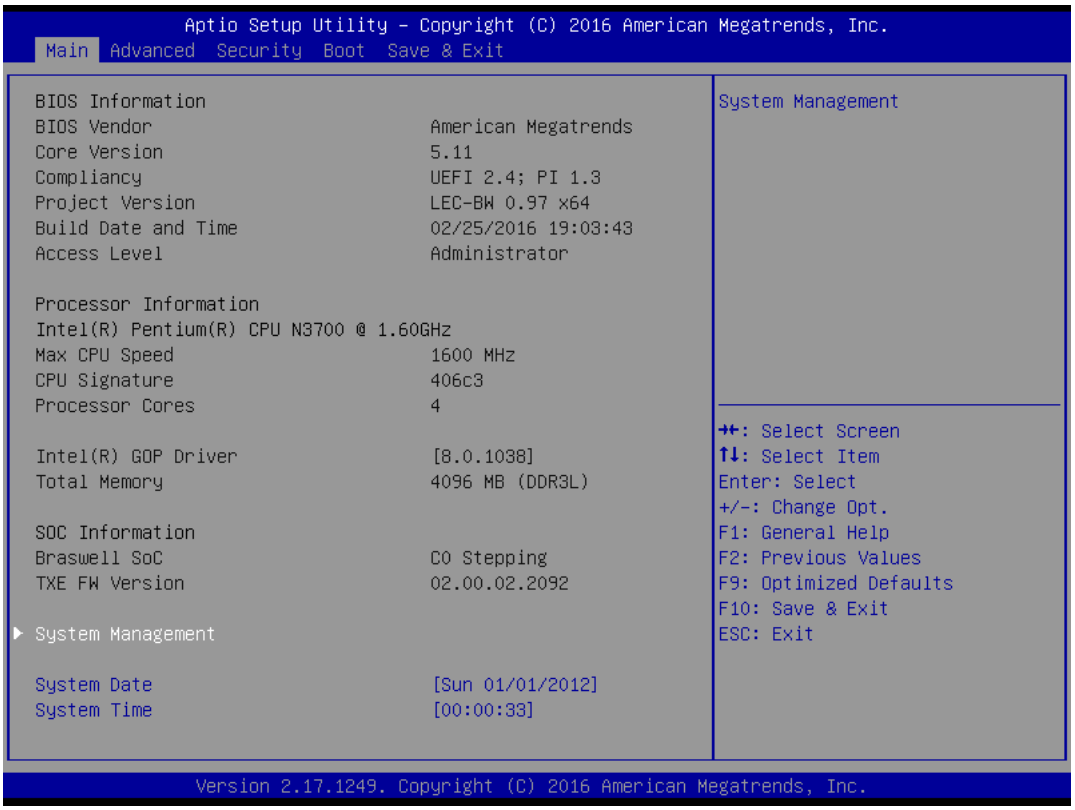


Figure 4-1: BIOS Setup Main Menu

Main Menu > System Information

Table 4-2: Main Menu > System Information

Feature	Options	Description
• Project Version	• Info only	• ADLINK BIOS version
• Build Date and Time	• Info only	• Date the BIOS was built

Main Menu > Processor Information

Table 4-3: Main Menu > Processor Information

Feature	Options	Description
• CPU Brand String	• Info only	• Display CPU brand name
• Max CPU Speed	• Info only	• Display CPU frequency
• CPU Signature	• Info only	• Display CPU ID
• Processors Cores	• Info only	• Display number of processor

Main Menu > VGA Firmware Version

Table 4-4: Main Menu > VGA Firmware Version

Feature	Options	Description
• IGFX VBIOS Version • IGFX GOP Version	• Info only	• Display legacy VBIOS or GOP driver version

Main Menu > Memory Information

Table 4-5: Main Menu > Memory Information

Feature	Options	Description
• Total Memory	• Info only	• Display total memory information

Main Menu > SOC Information

Table 4-6: Main Menu Main Menu > SOC Information

Feature	Options	Description
• Braswell Soc	• Info only	• Display SOC stepping
• TXE FW Version	• Info only	• Display version of TXE

Main Menu > System Management

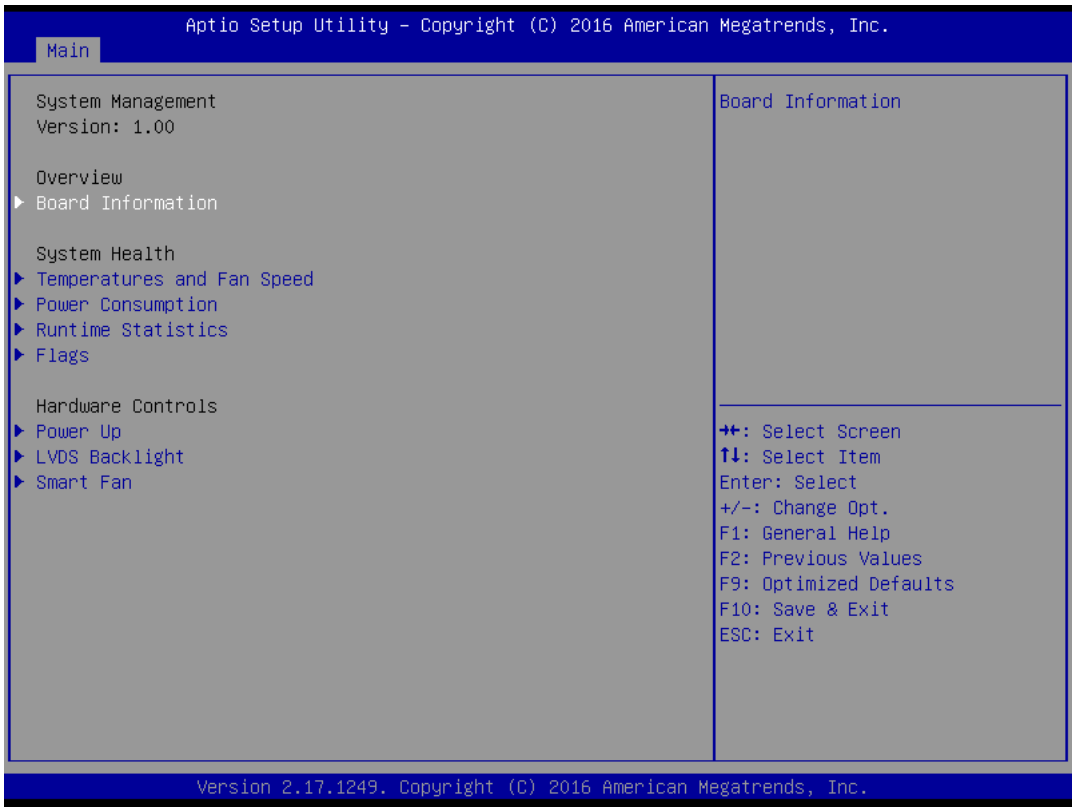


Figure 4-2: BIOS Setup Main Menu > System Management

Main Menu > System Management > Board Information

Table 4-7: Main Menu> System Management > Board Information

Board Information	Options	Description
• SEMA Firmware	• Read only	• Display SMC firmware
Build Date	• Read only	• Display SMC firmware build date
• SEMA Boot loader	• Read only	• Display SMC boot loader
Build Date	• Read only	• Display SMC boot loader build date
• Hardware Version	• Read only	• Display SMC hardware version
• Serial Number	• Read only	• Display SMC serial number
• Manufacturing Date	• Read only	• Display SMC manufacturing date
• Last Repair Date	• Read only	• Display SMC last repair date
• MAC ID	• Read only	• Display SMC MAC ID
• SEMA Features:	• Read only	• Display SEMA features

Main Menu > System Management > Temperatures and Fan Speed

Table 4-8: Main Menu > System Management > Temperature and Fan Speed

Feature	Options	Description
• Temperatures and Fan	• Info only	
Board Temperatures	• Info only	
▷ Current	• Read only	• Display current board temperature
▷ Startup	• Read only	• Display board startup temperature
▷ Min	• Read only	• Display board min. temperature
▷ Max	• Read only	• Display board max. temperature
CPU Fan Speed	• Read only	• Display CPU fan speed

Main Menu > System Management > Power Consumption

Table 4-9: Main Menu > System Management > Power Consumption

Feature	Options	Description
• Power Consumption	• Info only	
Current Input Current	• Read only	• Display input current
Current Input Power	• Read only	• Display input power
VCC_CORE	• Read only	• Display actual Core voltage
VNN_A	• Read only	• Display actual SOC voltage
VGG_S3	• Read only	• Display actual GFX Core voltage
VDDQ	• Read only	• Display actual Memory voltage
VRTC	• Read only	• Display actual RTC voltage
V3P3_S	• Read only	• Display actual System voltage
V5Vin	• Read only	• Display actual VIN voltage
VSMARC	• Read only	• Display actual SMARC voltage
V1P5_S0	• Read only	• Display actual V1.50 voltage

Table 4-9: Main Menu > System Management > Power Consumption (Continued)

V1P24_A	• Read only	• Display actual V1.24 voltage
V1P05_A	• Read only	• Display actual V1.05 voltage
V1P15_S	• Read only	• Display actual V1.15 voltage
V1P8_A	• Read only	• Display actual V1.80 voltage
V3P3_A	• Read only	• Display actual V3.30 voltage

Main Menu > System Management > Runtime Statistics

Table 4-10: Main Menu > System Management > Runtime Statistics

Feature	Options	Description
• Runtime Statistics	• Info only	
Total Runtime	• Read only	• The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	• Read only	• The returned value specifies the time in seconds the system is running in S0 state. • This counter is cleared when the system is removed from the external power supply.
Power Cycles	• Read only	• The returned value specifies the number of times the external power supply has been shut down
Boot Cycles	• Read only	• The Bootcounter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	• Read only	• The boot reason is the event which causes the reboot of the system.

Main Menu > System Management > Flags

Table 4-11: Main Menu > System Management > Flags

Feature	Options	Description
• Flags	• Info only	
BMC Flags	• Read only	
BIOS Select	• Read only	• Display the selection of current BIOS ROM
ATX/AT-Mode	• Read only	• Display ATX/AT-Mode
Exception Code	• Read only	• System exception reason

Main Menu > System Management > Power Up

Table 4-12: Main Menu > System Management > Power Up

Feature	Options	Description
• Power Up	• Info only	
Power Up watchdog Note: F12 disables the Power Up Watchdog.	• Enabled • **Disabled**	• The Power-Up Watchdog resets the system after a certain amount of time after power-up.
Power-up Mode Attention: The Power-Up Mode only has affect, if the module is in ATX-Mode.	• **Turn on** • Remain off • Last State	• Turn On: The machine starts automatically when the power supply is turned on. • Remain Off: To start the machine the power button has to be pressed. • Last State: When powered on during a power failure the system will automatically power on when power is restored.

Main Menu > System Management > LVDS Backlight

Table 4-13: Main Menu > System Management > LVDS Backlight

Feature	Options	Description
• LVDS Backlight	• Info only	
LVDS Backlight Bright	• 255	• The value range starts at 0 and ends at 255.

Main Menu > System Management > Smart Fan

Table 4-14: Main Menu > System Management > Smart Fan

Feature	Options	Description
CPU Fan Mode	• **AUTO (Smart Fan)** • Fan Off • Fan On	• Select CPU fan mode
CPU Trigger Point 1	• Read only	
▷ Trigger Temperature	• 40	• Specifies the temperature threshold at which the BMC turns on the CPU fan with the specified PWM level
▷ PWM Level	• 30	• Select PWM level
CPU Trigger Point 2	• Read only	
▷ Trigger Temperature	• 50	• Specifies the temperature threshold at which the BMC turns on CPU fan the specified PWM level
▷ PWM Level	• 40	• Select PWM level
CPU Trigger Point 3	• Read only	
▷ Trigger Temperature	• 60	• Specifies the temperature threshold at which the BMC turns on CPU fan the specified PWM level
▷ PWM Level	• 63	• Select PWM level
CPU Trigger Point 4	• Read only	

Table 4-14: Main Menu > System Management > Smart Fan (Continued)

▷ Trigger Temperature	• 70	• Specifies the temperature threshold at which the BMC turns on CPU fan the specified PWM level
▷ PWM Level	• 100	• Select PWM level

Main Menu > System Date and Time

Table 4-15: Main Menu > System Date and Time

Feature	Options	Description
• System Date	• Day of Week, MM/DD/YYYY	• Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)
• System Time	• HH/MM/SS	• Presented as a 24-hour clock setting in hours, minutes, and seconds

4.1.3 Advanced Menu

This menu contains the settings for most of the user interfaces in the system. The “Advanced” menu provides configuration settings for CPU, Memory, Graphics, SATA, USB, Network, Audio, PCIe Configuration, ACPI Power Management, Serial Console, Thermal, and Miscellaneous.

Inappropriate values for any of the following advanced settings below may cause system errors.

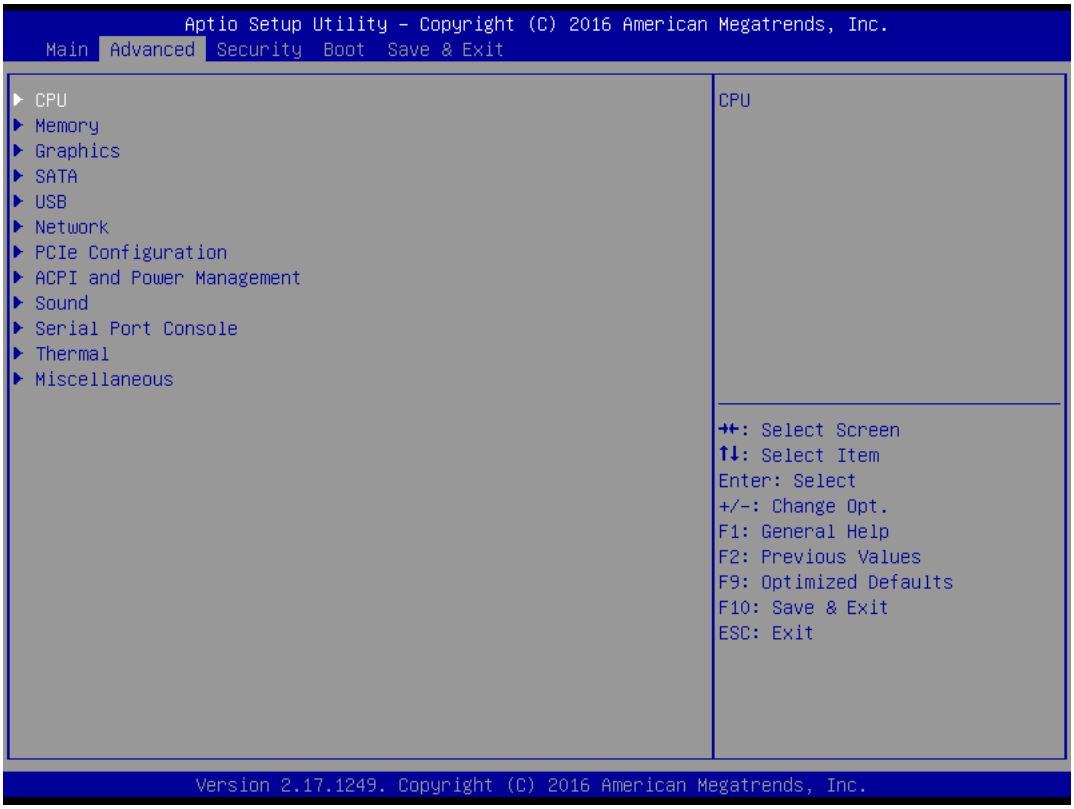


Figure 4-3: BIOS Setup Advanced Menu

Advanced Menu > CPU

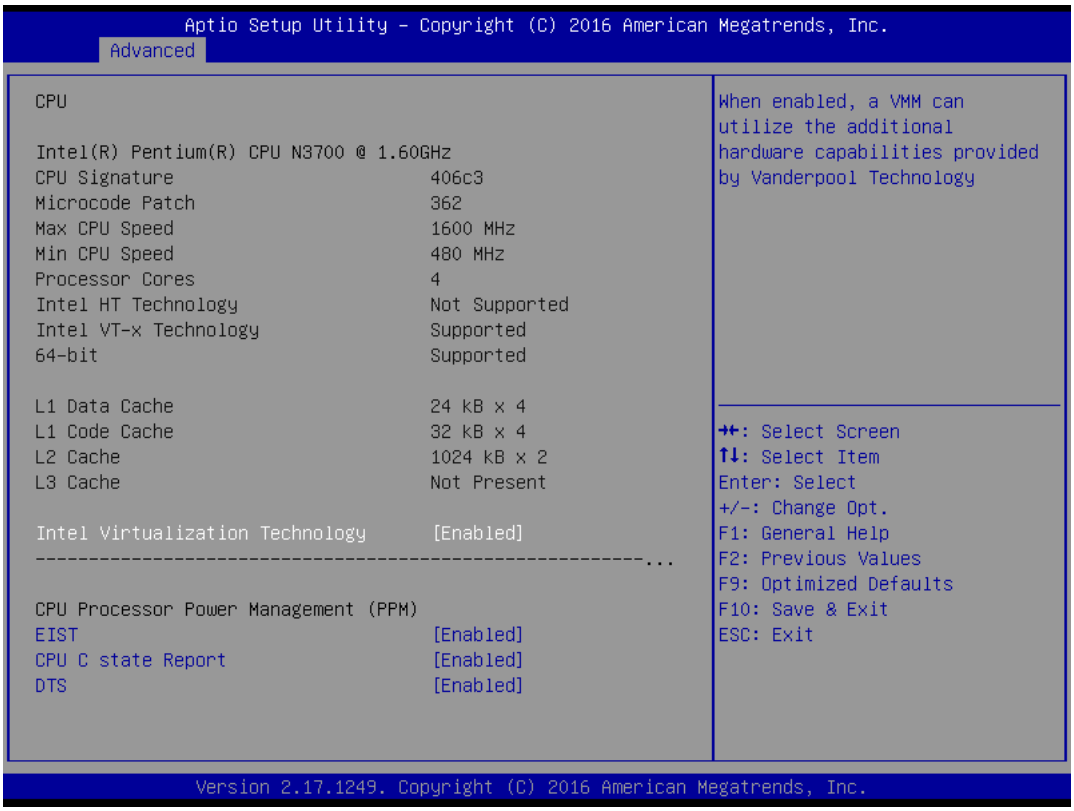


Figure 4-4: BIOS Setup Advanced Menu > CPU

Table 4-16: Advanced Menu > CPU

Feature	Options	Description
• CPU	• Info only	
• CPU Brand Name	• Info only	• Display CPU brand name
• CPU Signature	• Info only	• Display CPU signature
• Microcode Patch	• Info only	• Display microcode patch
• Max CPU speed	• Info only	• Display max. CPU speed
• Min CPU speed	• Info only	• Display min. CPU speed
• Processor Cores	• Info only	• Display number of processor cores
• Intel HT Technology	• Info only	• Display Intel HT Technology support
• Intel VT-x Technology	• Info only	• Display Intel VT-x Technology support
• 64-bit	• Info only	• Display 64-bit support
• L1 Data Cache	• Info only	• Display cache info
• L1 Code Cache	• Info only	• Display cache info
• L2 Cache	• Info only	• Display cache info
• L3 Cache	• Info only	• Display cache info
• Intel Virtualization Technology	• Disabled • **Enabled**	• When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Table 4-16: Advanced Menu > CPU (Continued)

• CPU Processor Power Management (PPM)	• Info only	
• EIST	• Disabled • **Enabled**	• Enable/Disable Intel SpeedStep
• CPU C state Report	• Disabled • **Enabled**	• Enable/Disable CPU C state report to OS
• DTS	• Disabled • **Enabled**	• Enabled/Disable digital thermal sensor

Advanced Menu > Memory

Figure 4-5: BIOS Setup Advanced Menu > Memory

Table 4-17: Advanced Menu > Memory

Feature	Options	Description
• Memory	• Info only	
• Total Memory	• Info only	• Display total memory
• Memory Frequency	• Info only	• Display memory frequency
• Memory Voltage	• Info only	• Display memory vlotage
• Memory Slot0	• Info only	• Display DIMM#0
• SPD Write Protect	• **Enabled** • Disabled	• Enabled: Writes to SMBus slave addresses A0h – Aeh are disabled

Table 4-17: Advanced Menu > Memory (Continued)

• Max TOLUD	• **2 GB** • 2.25 GB • 2.5 GB • 2.75 GB • 3 GB	• Maximum value of TOLUD

Advanced Menu > Graphics

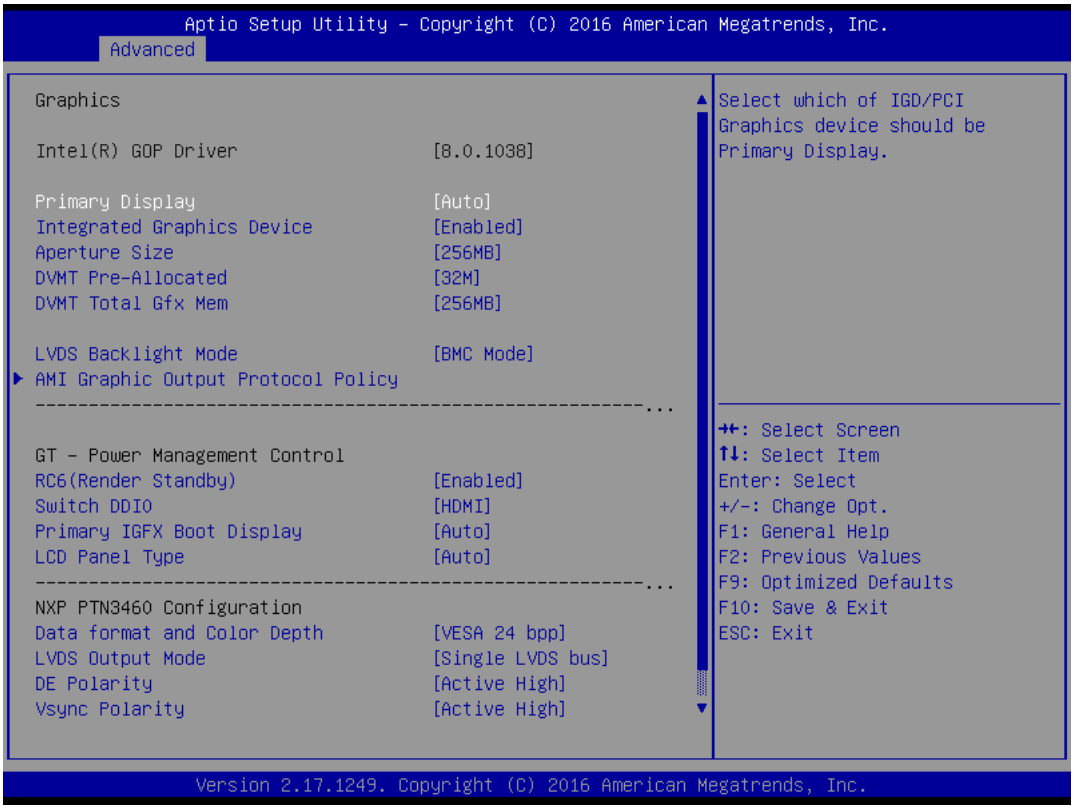


Figure 4-6: BIOS Setup Advanced Menu > Graphics

Table 4-18: Advanced Menu > Graphics

Feature	Options	Description
• Graphics	• Info only	
• IGFX VBIOS Version	• Info only	
• Primary Display	• **Auto** • IGD • PCIE	• Select which graphics device (IGD/ PCI) should be primary display
• Integrated Graphics Device	• **Enabled** • Disabled	• Enabled: Enable Integrated Graphics Device (IGD) when selected as the primary display; Disabled: Always disable IGD
• Aperture Size	• **256MB**	• Select the aperture size
• DVMT Pre-Allocated	• **32M**	• Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.

Table 4-18: Advanced Menu > Graphics (Continued)

• DVMT Total Gfx Mem	• **256MB**	• Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.
• LVDS Backlight Mode	• **BMC Mode** • GTT Mode	• Select LVDS backlight control function.
• AMI Graphics Output Protocol Policy • [UEFI GOP only]	• Submenu	• User select monitor output by graphics output protocol
• GT – Power Management Control	• Info only	
• RC6 (Render Standby)	• **Enabled** • Disabled	• Enable/Disable render standby support
• Switch DDI0	• **HDMI** • Display Port	• DDI0 function choose to Display Port or HDMI
• Primary IGFX Boot Display	• **Auto** • EFP • LFP • EFP2	• Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display
• LCD Panel Type	• **Auto**	• Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.
• NXP PTN3460 Configuration	• Info only	
• Data format and Color Depth	• **VESA 24 bpp** • JEIDA 24 bpp • JEIDA/vesa 18 bpp	• Data format and Color Depth select
• LVDS Output Mode	• Dual LVDS bus • **Single LVDS bus**	• Single/Dual mode select
• DE Polarity	• **Active High** • Active Low	• DE Polarity select
• Vsync Polarity	• **Active High** • Active Low	• Vsync Polarity select
• Hsync Polarity	• **Active High** • Active Low	• Hsync Polarity select

Advanced Menu > AMI Graphics Output Protocol Policy

Table 4-19: Advanced Menu > AMI Graphics Output Protocol Policy

Feature	Options	Description
• Intel(R) Valley View Graphics Controller	• Info only	
• Intel(R) GOP Driver	• Info only	
• Output Select [List connect device]	• HDMI1	• Output Interface.
• Brightness Setting [LFP device connect only]	• 255	• Set GOP Brightness value.
• BIST Enable	• Enabled • **Disabled**	• Starts or stops the built-in self-test (BIST) on the integrated display panel.

Advanced Menu > SATA

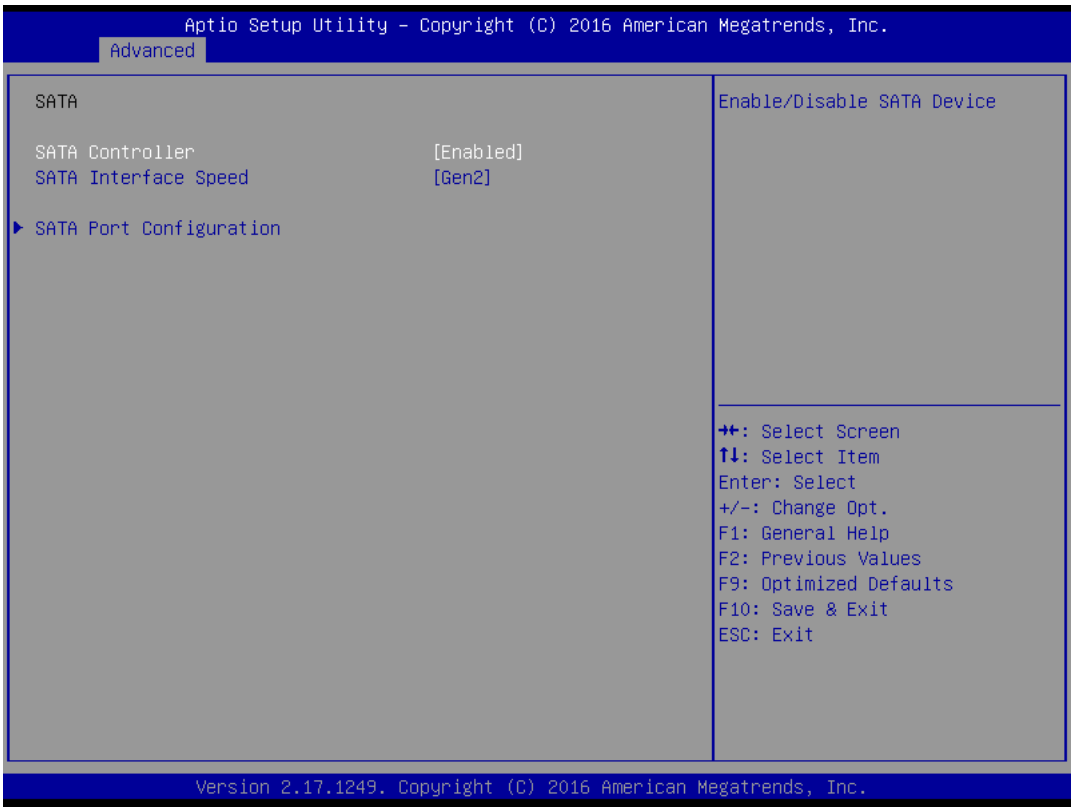


Figure 4-7: BIOS Setup Advanced Menu > SATA

Table 4-20: Advanced Menu > SATA

Feature	Options	Description
• SATA	• Info only	
• SATA Controller(s)	• **Enabled** • Disabled	• Enable/Disable SATA Device.
• SATA Interface Speed	• Gen1 • **Gen2** • Gen3	• Select SATA Interface speed, CHV A1 always with Gen1 Speed.
• SATA Port Configuration	• Submenu	

Advanced Menu > SATA > SATA Port Configuration

Table 4-21: Advanced Menu > SATA > SATA Port Configuration

Feature	Options	Description
• SATA Port Configuration	• Info only	
• Port X	• Disabled • **Enabled**	• Enable/Disable SATA port X.
• Spin Up Device	• Enabled • **Disabled**	• If enabled for any of ports, Staggered Spin Up will be performed, and only the drives that have this option enabled will spin up at boot. Otherwise, all drives spin up at boot.

Table 4-21: Advanced Menu > SATA > SATA Port Configuration (Continued)

• Device Sleep Support	• Enabled • **Disabled**	• Enable/Disable Device Sleep Support on that port.
• HotPlug	• **Enabled** • Disabled	• Enable/Disable SATA port X hotplug.

Advanced Menu > USB

Figure 4-8: BIOS Setup Advanced Menu > USB

Table 4-22: Advanced Menu > USB

Feature	Options	Description
• USB	• Info only	
• USB Module Version	• Info only	
• USB Devices	• Info only	• Drives, keyboards, mouse, hubs
• Legacy USB Support	• **Enabled** • Disabled • Auto	• Enables legacy USB support. • Auto option disables legacy support if no USB devices are connected. • Disable option will keep USB devices available only for EFI applications and setup.
• XHCI Hand-off	• Enabled • **Disabled**	• This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI OS driver.
• USB Mass Storage Driver Support	• **Enabled** • Disabled	• Enable/Disable USB mass storage driver support.

Table 4-22: Advanced Menu > USB (Continued)

• Port 60/64 Emulation	• Disabled • **Enabled**	• Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.
• USB Configuration	• Submenu	
• USB hardware delays and time-outs:	• Info only	
• USB transfer time-out	• 1 sec • 5 sec • 10 sec • **20 sec**	• The time-out value for control, bulk, and interrupt transfers
• Device reset time-out	• 10 sec • **20 sec** • 30 sec • 40 sec	• USB mass storage device Start Unit command time-out.
• Device power-up delay	• **Auto** • Manual	• Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.
• Mass Storage Devices	• Info only	• List current USB mass storage devices.

Advanced Menu > USB > USB Configuration

Table 4-23: Advanced Menu > USB > USB Configuration

Feature	Options	Description
• USB Configuration	• Info only	
• XHCI Mode	• **Enabled** • Disabled	• Mode of operation of xHCI controller.

Advanced Menu > Network

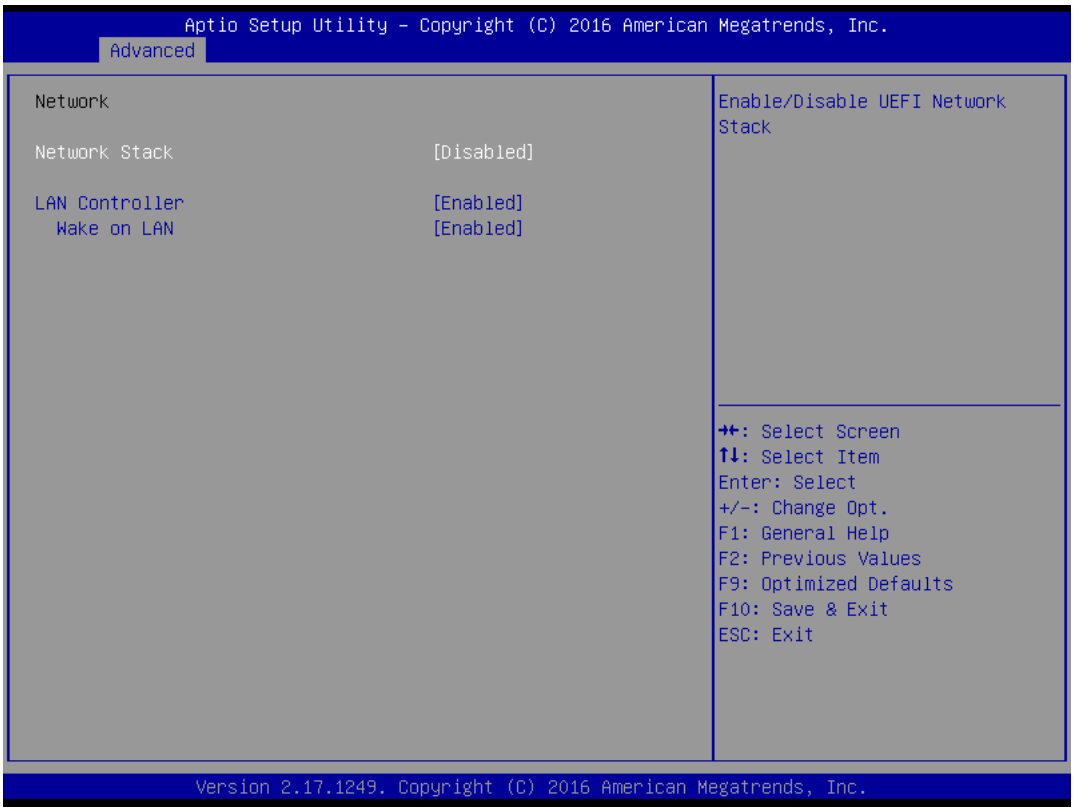


Figure 4-9: BIOS Setup Advanced Menu > Network

Table 4-24: Advanced Menu > Network

Feature	Options	Description
• Network	• Info only	
• Network Stack	• Enabled **Disabled**	• Enable/Disable UEFI network stack.
• LAN Controller	• **Enabled** Disabled	• Enable/Disable LAN controller.
• Wake on LAN	• Disable • **Enabled**	• If Enabled: LAN_PWR is always on; If Disabled: LAN_PWR is off after entering Suspend mode.

Advanced Menu > PCIe Configuration

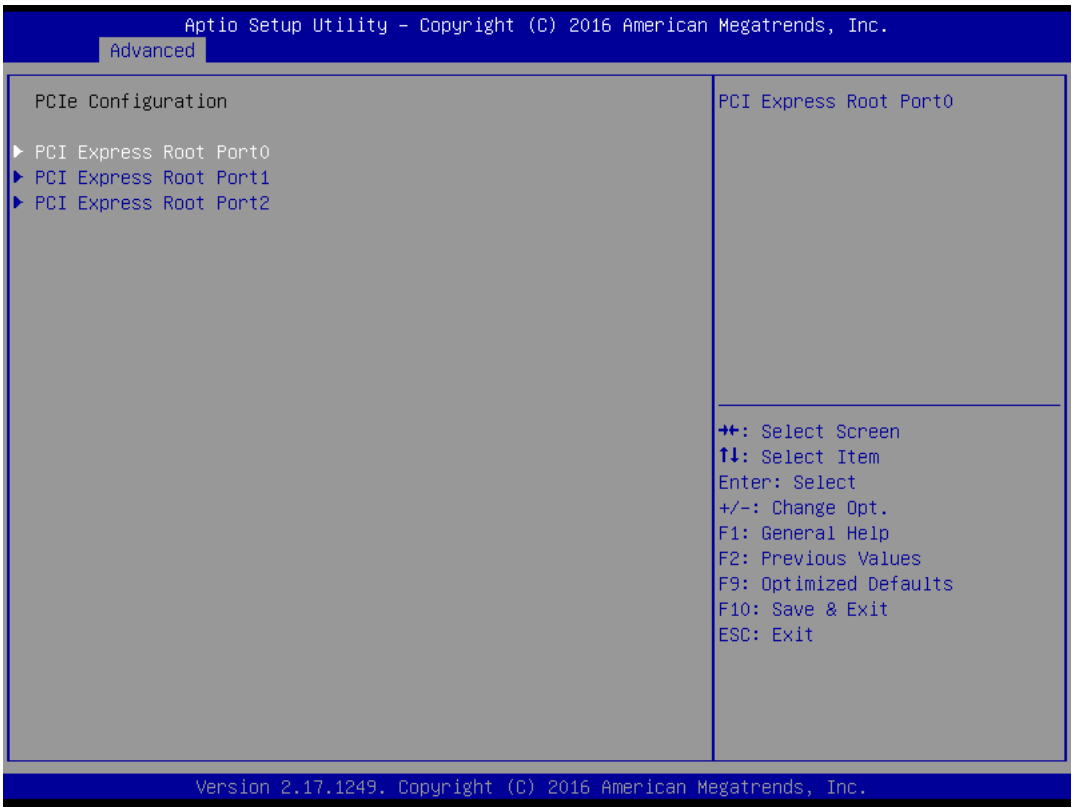


Figure 4-10: BIOS Setup Advanced Menu > PCIe Configuration

Table 4-25: Advanced Menu > PCIe Configuration

Feature	Options	Description
• PCIe Configuration	• Info only	
• PCI Express Root Port x	• Submenu	

Advanced Menu > PCIe Configuration > PCI Express Port x

Table 4-26: Advanced Menu > PCIe Configuration > PCI Express Port x

Feature	Options	Description
• PCI Express Port x	• **Enabled** • Disabled	• Control the PCI Express Root Port.
• ASPM	• Auto • **Disabled** • L0s • L1 • L0sL1	• PCI Express Active State Power Management settings.
• URR	• **Disabled** • Enabled	• PCI Express Unsupported Request Reporting Enable/Disable.
• FER	• **Disabled** • Enabled	• PCI Express Device Fatal Error Reporting Enable/Disable.
• NFER	• **Disabled** • Enabled	• PCI Express Device Non-Fatal Error Reporting Enable/Disable.

Table 4-26: Advanced Menu > PCIe Configuration > PCI Express Port x (Continued)

• CER	• **Disabled** • Enabled	• PCI Express Device Correctable Error Reporting Enable/Disable.
• SEFE	• **Disabled** • Enabled	• Root PCI Express System Error on Fatal Error Enable/Disable.
• SENFE	• **Disabled** • Enabled	• Enable or disable Root PCI Express System Error on Non-Fatal Error.
• SECE	• **Disabled** • Enabled	• Root PCI Express System Error on Correctable Error Enable/Disable.
• PME SCI	• Disabled • **Enabled**	• PCI Express PME SCI Enable/ Disable.
• Hot Plug	• Disabled • **Enabled**	• Enable or disable PCI Express hotplug.
• PCIe Speed	• **Auto** • Gen 2 • Gen 1	• Configure PCIe port speed.

Advanced Menu > ACPI and Power Management

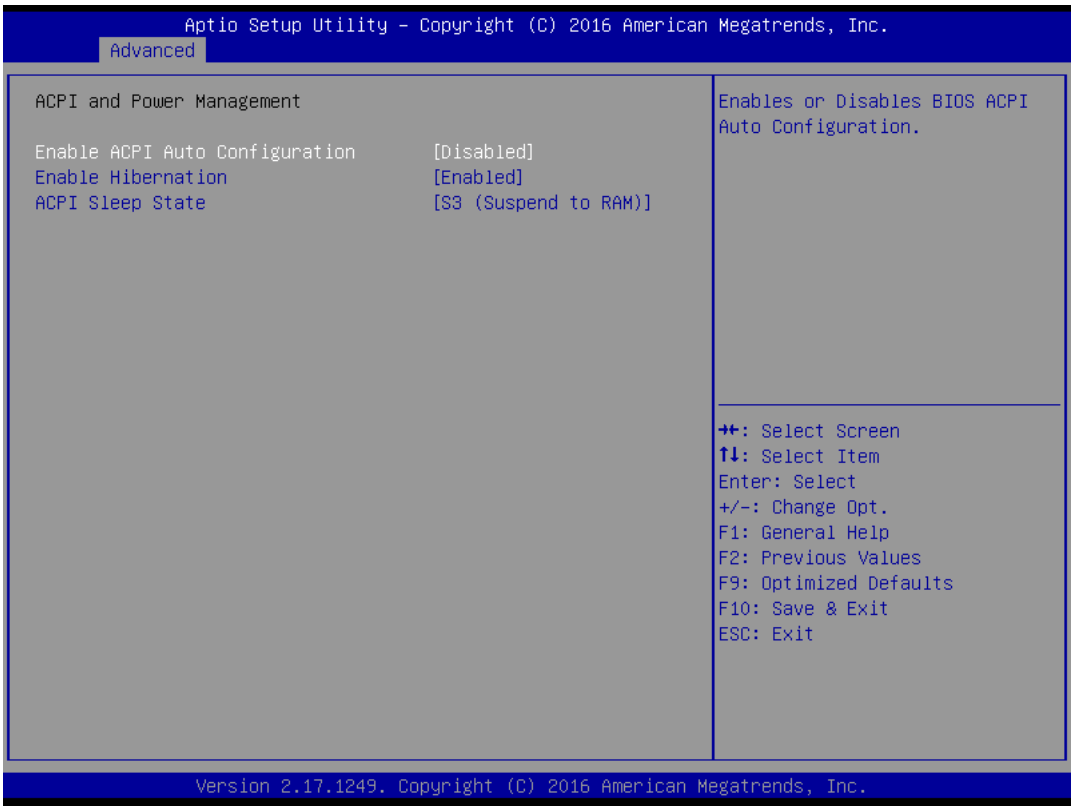


Figure 4-11: BIOS Setup Advanced Menu > ACPI and Power Management

Table 4-27: Advanced Menu > ACPI and Power Management

Feature	Options	Description
• ACPI and Power Management	• Info only	
• Enable ACPI Auto Configuration	• Enabled **Disabled**	• Enables or disables BIOS ACPI Auto Configuration.

Table 4-27: Advanced Menu > ACPI and Power Management (Continued)

• Enable Hibernation	• **Enabled** Disabled	• Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
• ACPI Sleep State	• Suspend Disabled • **S3 (Suspend to RAM)**	• Select the highest ACPI sleep state the system will enter when the Suspend button is pressed.

Advanced Menu > Sound

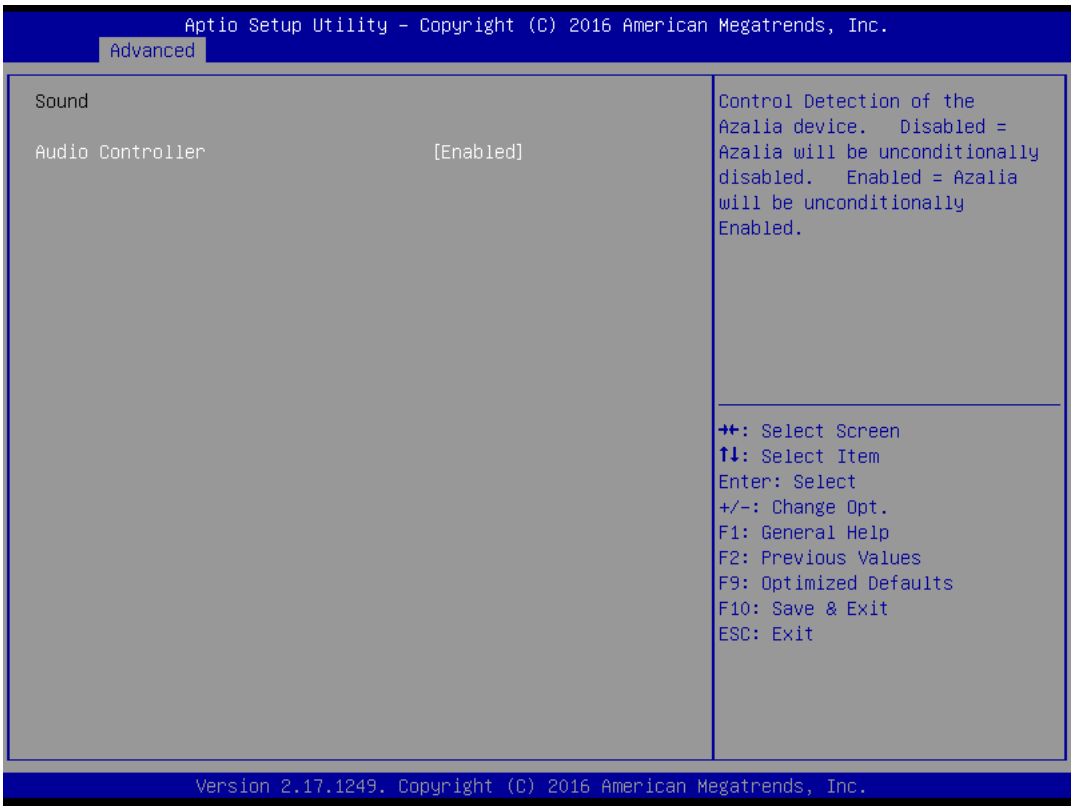


Figure 4-12: BIOS Setup Advanced Menu > Sound

Table 4-28: Advanced Menu > Sound

Feature	Options	Description
• Sound	• Info only	
• Audio Controller	• Disabled • **Enabled**	• Control Detection of the Azalia device. Disabled = Azalia will be unconditionally disabled. Enabled = Azalia will be unconditionally Enabled.

Advanced Menu > Serial Port Console

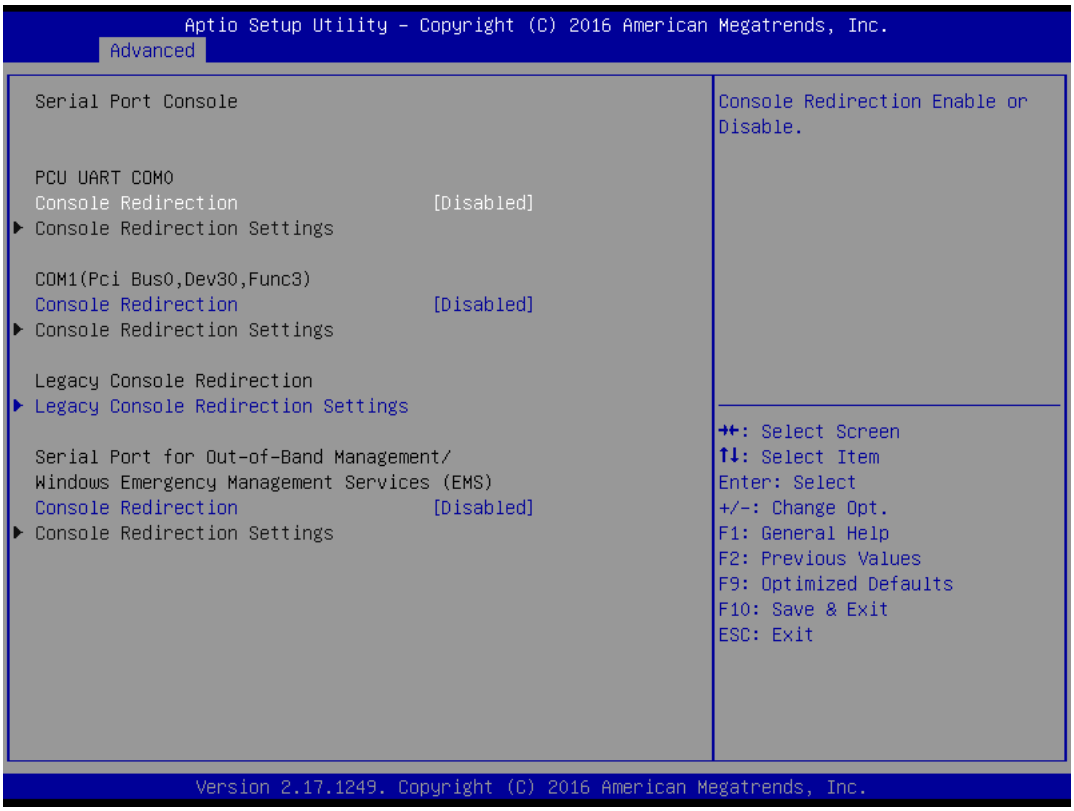


Figure 4-13: BIOS Setup Advanced Menu > Serial Port Console

Table 4-29: Advanced Menu > Serial Port Console

Feature	Options	Description
• Serial Port Console	• Info only	
• PCU UART COM0	• Info only	
▶ Console Redirection	• **Disabled** • Enabled	• Console Redirection enable or disable.
▶ Console Redirection Settings	• Submenu	• The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
• COM1 (Pci Bus0,Dev30,Func3)	• Info only	
▶ Console Redirection	• **Disabled** • Enabled	• Console Redirection enable or disable.
▶ Console Redirection Settings	• Submenu	• The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
▶ Legacy Console Redirection	• Info only	

Table 4-29: Advanced Menu > Serial Port Console (Continued)

▶ Legacy Console Redirection Settings	• Submenu	
• Serial Port for Out-of-Band • Management/Windows Emergency • Management Services (EMS)	• Info only	
▶ Console Redirection	• **Disabled** • Enabled	• Console Redirection enable or disable.
▶ Console Redirection Settings	• Submenu	• The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

Advanced Menu > Serial Port Console > Console Redirection Settings (COM0 / COM1)

Table 4-30: Advanced Menu > Serial Port Console > Console Redirection Settings (COM0 / COM1)

Feature	Options	Description
• COM0/COM1 • Console Redirection Settings	• Info only	
• Terminal Type	• VT100 • VT100+ • VT-UTF8 • **ANSI**	• VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes. ANSI: Extended ASCII char set.
• Bits per second	• 9600 • 19200 • 38400 • 57600 • **115200**	• Selects serial port transmission speed. The speed must be matched on the remote computer. Long or noisy lines may require lower speeds.
• Data Bits	• 7 • **8**	• Select data bits.
• Parity	• **None** • Even • Odd • Mark • Space	• Select parity.
• Stop Bits	• **1** • 2	• Select number of stop bits.
• Flow Control	• **None** • Hardware RTS/CTS	• Select flow control.
• VT-UTF8 Combo Key Support	• Disabled • **Enable**	• Enable VT-UTF8 combination key support for ANSI/VT100 terminals.
• Recorder Mode	• **Disabled** • Enable	• With this mode enabled only text will be sent. This is to capture terminal data.
• Resolution 100x31	• **Disabled** • Enable	• Enables or disables extended terminal resolution
• Legacy OS Redirection	• **80x24** • 80x25	• On legacy OSes, the number of rows and columns supported by redirection

Table 4-30: Advanced Menu > Serial Port Console > Console Redirection Settings (COM0 / COM1) (Continued)

• Putty KeyPad	• **VT100** • LINUX • XTERMR6 • SCO • ESCN • VT400	• Select FunctionKey and KeyPad on Putty.
• Redirection After BIOS Post	• **Always Enabled** • BootLoader	• The Settings specify if BootLoader is selected, then legacy console redirection is disabled before booting to legacy OS. Default value is Always Enable which means legacy console redirection is enabled for legacy OS.

Advanced Menu > Serial Port Console > Legacy Console Redirection Settings (COM1)

Table 4-31: Advanced Menu > Serial Port Console > Legacy Console Redirection Settings (COM1)

Feature	Options	Description
• Legacy Serial Redirection Port	• **PCU UART COM0** • COM1(Pci Bus0,Dev30,Func3)	• Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages

Advanced Menu > Serial Port Console > Console Redirection Settings (EMS)

Table 4-32: Advanced Menu > Serial Port Console > Serial Port Console Redirection Settings (EMS)

Feature	Options	Description
• Out-of-Band Mgmt Port	• **PCU UART COM0** • COM1(Pci Bus0,Dev30,Func3)	• Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.
• Terminal Type	• VT100 • VT100+ • **VT-UTF8** • ANSI	• VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.
• Bits per second	• 9600 • 19200 • 57600 • **115200**	• Selects serial port transmission speed. The speed must be matched on the remote computer. Long or noisy lines may require lower speeds.
• Flow Control	• **None** • Hardware RTS/CTS • Software Xon/Xoff	• Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
• Data Bits	• Info only	
• Parity	• Info only	

Table 4-32: Advanced Menu > Serial Port Console > Serial Port Console Redirection Settings (EMS)

• Stop Bits	• Info only

Advanced Menu > Thermal

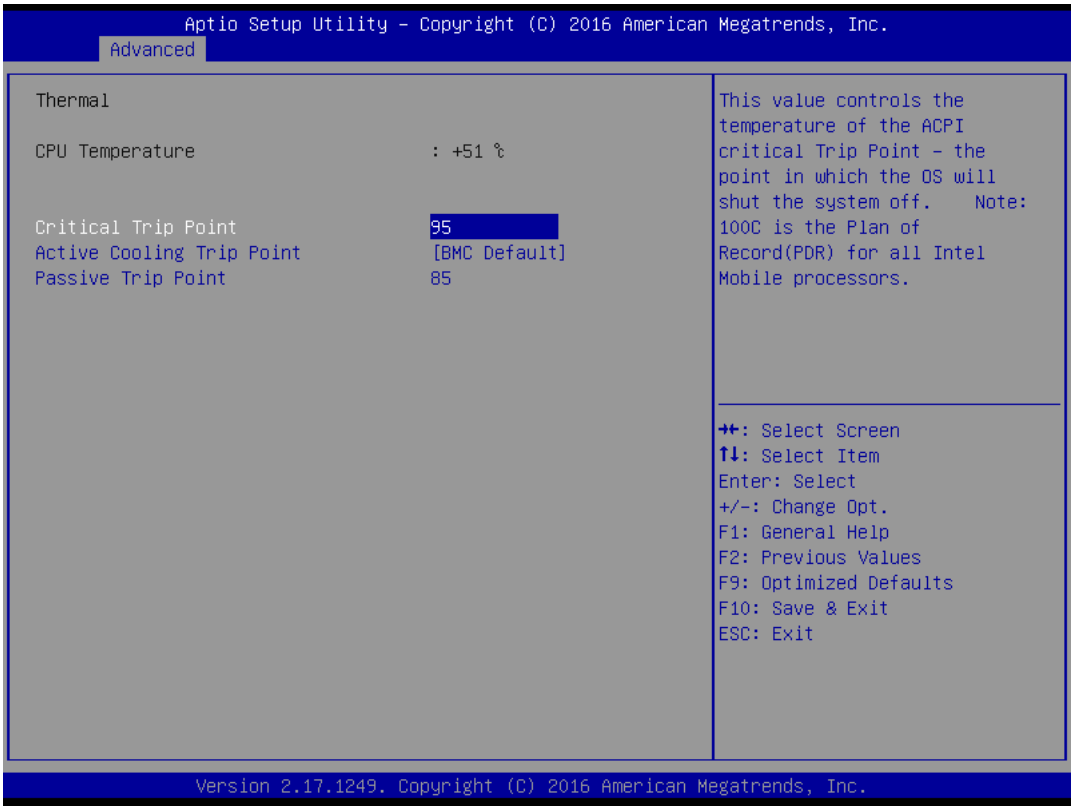


Figure 4-14: BIOS Setup Advanced Menu > Thermal

Table 4-33: Advanced Menu > Thermal

Feature	Options	Description
• Thermal	• Info only	
• CPU Temperature	• Info only	
• Critical Trip Point	• **Disabled** • 85 C • 95 C	• This value controls the temperature of the ACPI critical Trip Point - the point in which the OS will shut the system off. Note: 100C is the Plan of Record (PDR) for all Intel Mobile processors.
• Active Cooling Trip Point	• Disabled • 40 C • 50 C • 60 C • 70 C • **BMC Default**	• Active Cooling Trip Point.
• Passive Trip Point	• **Disabled** • 90 C • 80 C	• This value controls the temperature of the ACPI critical Trip Point - the point in which the OS will begin throttling the processor.

Advanced Menu > Miscellaneous

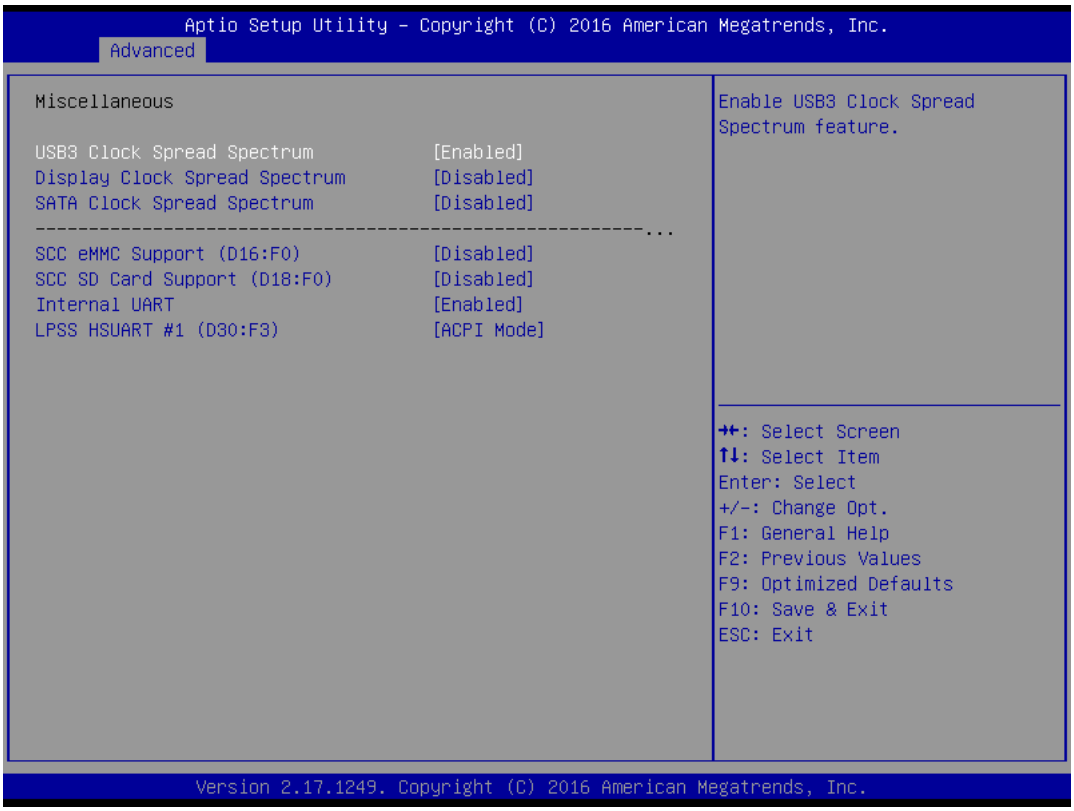


Figure 4-15: BIOS Setup Advanced Menu > Miscellaneous

Table 4-34: Advanced Menu > Miscellaneous

Feature	Options	Description
• Miscellaneous	• Info only	
• USB3 Clock Spread Spectrum	• **Enabled** • Disabled	• Enable USB3 Clock Spread Spectrum feature.
• Display Clock Spread Spectrum	• Enabled • **Disabled**	• Enable DISPLAY Clock Spread Spectrum feature.
• SATA Clock Spread Spectrum	• Enabled • **Disabled**	• Enable SATA Clock Spread Spectrum feature.
• SCC eMMC Support (D16:F0)	• ACPI mode • PCI mode • **Disable**	• SCC eMMC support enable/disable.
• SCC SD Card Support (D18:F0)	• ACPI mode • PCI mode • **Disable**	• SCC SD card support enable/ disable.
• Internal Uart	• Disabled • **Enable**	• Enable/Disable Internal UART
• LPSS HSUART #1 (D30:F3)	• **ACPI mode** • PCI mode • Disable	• Enable/Disable LPSS HSUART #1 Support

4.1.4 Security Menu

The Security menu allows you to set User and Administrator system passwords and to retrieve secure boot information.

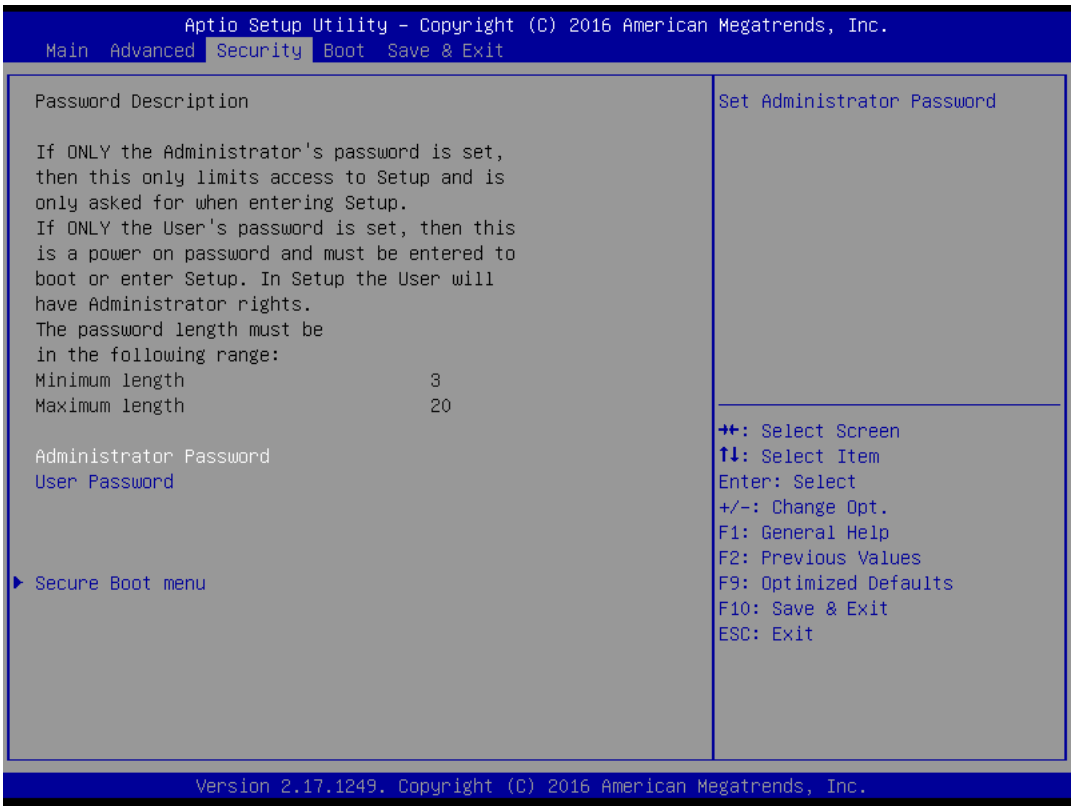


Figure 4-16: BIOS Setup Security Menu

Security Menu > Password Description

Table 4-35: Security Menu > Password Description

Feature	Options	Description
• Administrator Password	• Enter password	
• User Password	• Enter password	
• Secure Boot menu	• Submenu	• Customizable Secure Boot settings.

Security Menu > Secure Boot

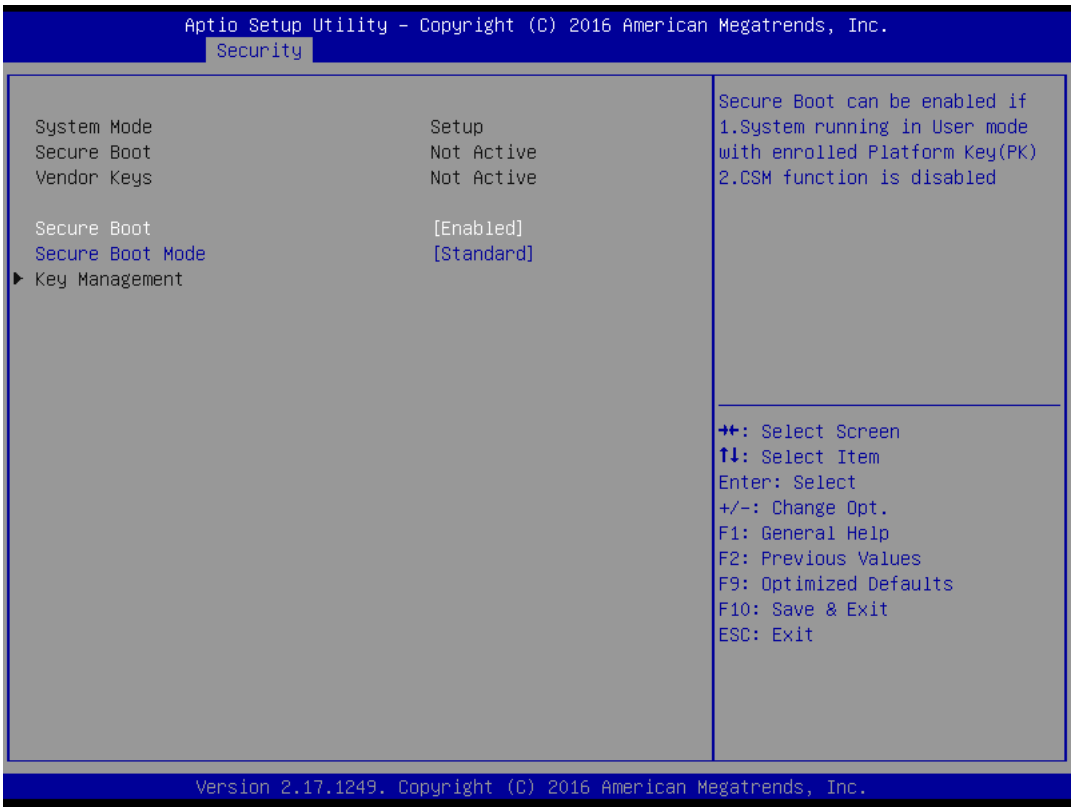


Figure 4-17: BIOS Setup Security Menu > Secure Boot

Table 4-36: Security Menu > Secure Boot

Feature	Options	Description
• System Mode	• Info only	
• Secure Boot	• Info only	
• Vendor Keys	• Info only	
• Secure Boot	• Disabled • **Enabled**	• Secure Boot can be enabled if: 1. System running in User mode with enrolled Platform Key (PK) 2. CSM function is disabled.
• Secure Boot Mode	• **Standard** • Custom	• Secure Boot mode selector. 'Custom' Mode enables users to change Image Execution policy and manage Secure Boot keys.

4.1.5 Boot Menu

The Boot menu allows you to configure how your system will boot and select the storage location from which the system boot up will occur.

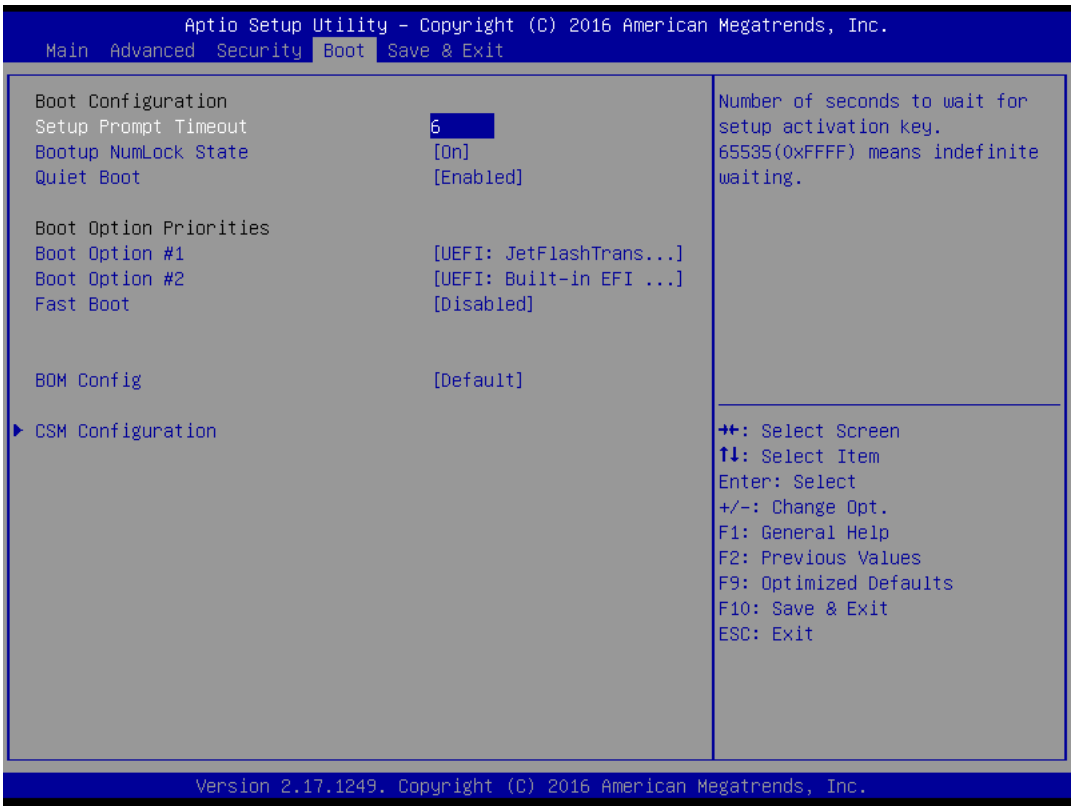


Figure 4-18: BIOS Setup Boot Menu

Table 4-37: BIOS Setup Boot Menu

Feature	Options	Description
• Boot Configuration	• Info only	
• Setup Prompt Timeout	• **6**	• Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
• Bootup NumLock State	• **On** • Off	• Select the keyboard NumLock state.
• Quiet Boot	• Disabled • **Enabled**	• Enable or disables logo Quiet Boot option for OEM Logo function.
• Boot Option Priorities	• Info only	
• Fast Boot	• **Disabled** • Enabled	• Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect on BBS boot options.
• BOM Config	• **Default** • Legacy System • Yocto Linux	• BOM Config
• CSM Configuration	• Submenu	• CSM configuration: Enable/Disable, Option ROM execution settings, etc.

Boot Menu > CSM Configuration

If more than one drive is attached to the LEC-BW, you can select from the “Boot Configuration” screen the boot order in which the drives are scanned for a bootable OS image.

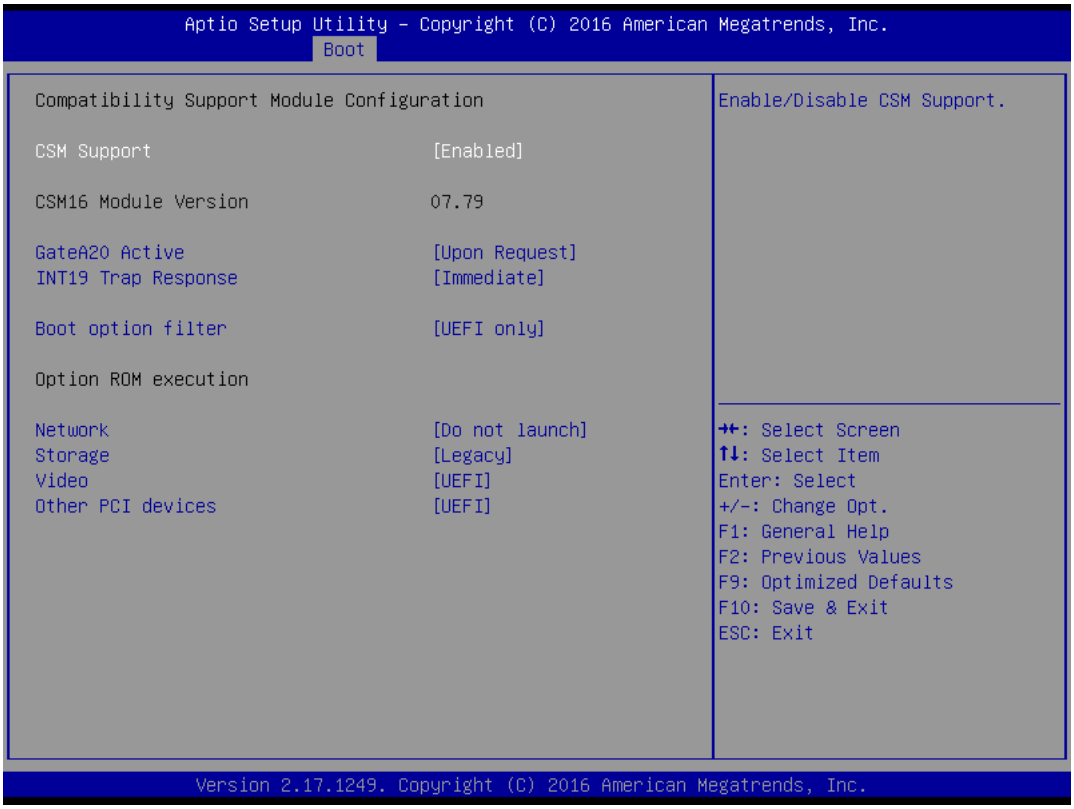


Figure 4-19: Boot Menu > CSM Configuration

Table 4-38: Boot Menu > CSM Configuration

Feature	Options	Description
• Compatibility Support Module Configuration	• Info	
• CSM Support	• **Enabled** • Disable	• CSM Support
• CSM16 Module Version	• Info only	
• GataA20 Active	• **Upon Request** • Always	• GataA20 Active
• INT19 Trap Response	• **Immediate** • Postponed	• INT19 Trap Response
• Boot option filter	• UEFI and Legacy • Legacy only • **UEFI only**	• Boot option filter
• Option ROM execution order	• Info only	
• Network	• **Do not launch** • UEFI only • Legacy only	• Controls the execution of UEFI and legacy PXE OpROM.
• Storage	• Do not launch • UEFI only • **Legacy only**	• Controls the execution of UEFI and legacy storage OpROM.

Table 4-38: Boot Menu > CSM Configuration (Continued)

• Video	• Do not launch • **UEFI only** • Legacy only	• Controls the execution of UEFI and legacy video OpROM.
• Other PCI devices	• **UEFI only** • Legacy only	• Determines OpROM execution policy for devices other than network, storage or video.

4.1.6 Save & Exit Menu

Use the Save and Exit menu to save or discard BIOS setting changes, restore or save setting defaults, and retrieve certain override information.

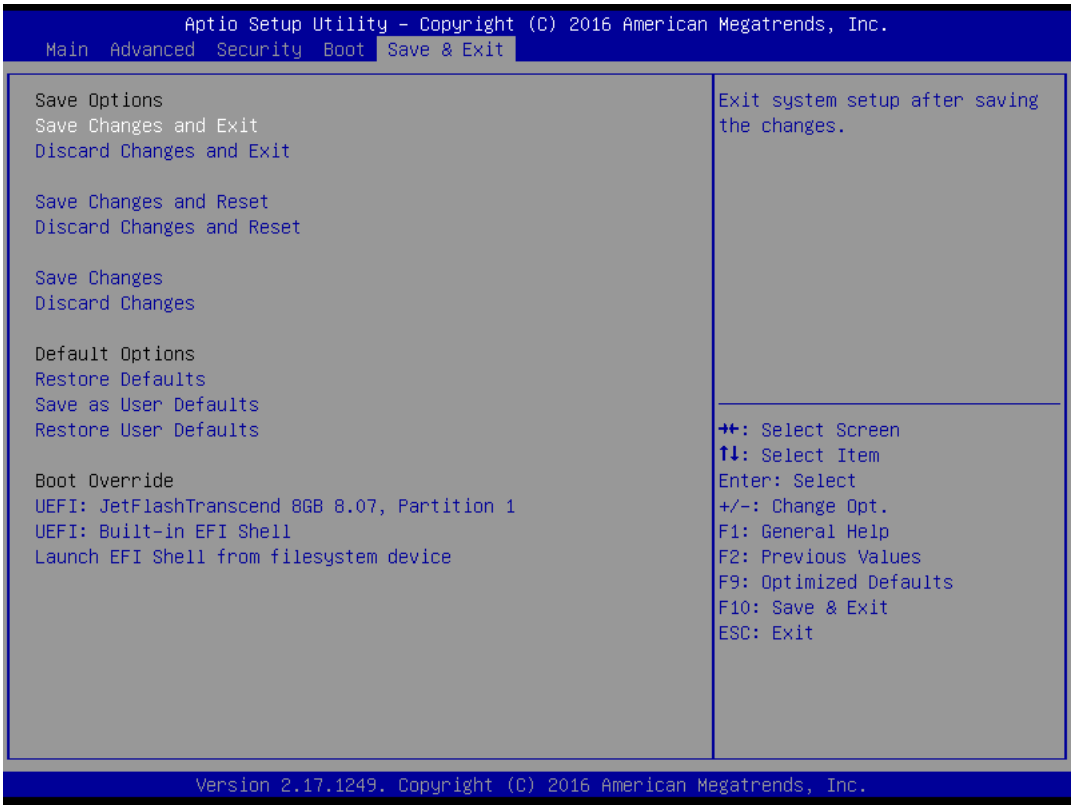


Figure 4-20: BIOS Setup Save and Exit Menu

Table 4-39: Save and Exit Menu

Feature	Options	Description
• Save Options	• Info only	
• Save Changes and Exit	Yes No	• Exit system setup after saving the changes.
• Discard Changes and Exit	Yes No	• Exit system setup without saving any changes.
• Save Changes and Reset	Yes No	• Reset the system after saving the changes.
• Discard Changes and Reset	Yes No	• Reset system setup without saving any changes.
• Save Changes	Yes No	• Save Changes done so far to any of the setup options.
• Discard Changes	Yes No	• Discard Changes done so far to any of the setup options.
• Default Options	• Info only	

Table 4-39: Save and Exit Menu (Continued)

• Restore Defaults	Yes No	• Restore/Load Default values for all the setup options.
• Save as User Defaults	Yes No	• Save the changes done so far as User Defaults.
• Restore User Defaults	Yes No	• Restore the User Defaults to all the setup options.
• Boot Override	• Info only	

4.2 SEMA functions

Under the management of the BMC chip (Board Management Controller), the SEMA utility (Smart Embedded Management Agent) provides system control and failure protection—counting, monitoring, and measuring hardware and software events, from which the SoC can trigger corrective commands. The optional SEMA Cloud utility not only controls local events on the module but system client events on the Internet of Things (IoT.) Refer to the following bullets for a list of SEMA functions.

- Total operating hours counter
  Counts the time the module has been run in minutes.
- On-time minutes counter
  Counts the seconds since last system start.
- Temperature monitoring of CPU and Board temperature
  Minimum and maximum temperature values of CPU and board are stored in flash.
- Power monitor
  Reads the current drawn by the board and reports the nominal operating voltage.
- Power cycles counter
- Boot counter
  Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
- Watchdog Timer
  Set / Reset / Disable Watchdog Timer.
- System Restart Cause
  Power loss / Watchdog / External Reset.
- Flash area
  1kB Flash area for customer data
- Protected Flash area
  128 Bytes for Keys, ID's, etc. can be stored in a write- and clear-protectable region.
- Board Identify
  Vendor / Board / Serial number

The SEMA Tools are available for Windows and Linux. SEMA functionality can also be used in applications. Refer to the SEMA software manual and technical manual on the ADLINK web site for more information.

4.2.1 Board Specific SEMA functions

Voltages

The BMC of the LEC-BW implements a Voltage Monitor and samples several Onboard Voltages. The Voltages can be read by calling the SEMA function, “Get Voltages”. The function returns a 16-bit value divided in Hi-Byte (MSB) and Lo-Byte (LSB).

Table 4-40: BMC Voltage Monitor Values

ADC Channel	Voltage Name	Voltage Formula [V]
0	---	---
1	+V1.0S	(MSB<<8 + LSB) * 3.3 / 1024
2	+V1.2S	(MSB<<8 + LSB) * 3.3 / 1024
3	+V1.8S	(MSB<<8 + LSB) * 3.3 / 1024
4	+V3.3S	(MSB<<8 + LSB) * 1.100 * 3.3 / 1024
5	+V1.5S	(MSB<<8 + LSB) * 3.3 / 1024
6	+V5.0A	(MSB<<8 + LSB) * 1.833 * 3.3 / 1024
7	(MAINCURRENT)	Use Main Current Function

Main Current

The BMC of the LEC-BW implements a Current Monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in Hi-Byte (MSB) and Lo-Byte (LSB). These four values represent the last four currents drawn by the board. The values are sampled every 250ms. The order of the four values is NOT in relationship to time. The access to the BMC may increase the drawn current of the whole system. In this case, you still have three samples without the influence of the read access.

Main Current = (MSB_n<<8 + LSB_n) * 8.06mA

TS#-Events

TS# is activated by a temperature sensor when a device reaches its critical temperature and released when the device is back in its normal temperature range. This counter gives the user information about temperature or cooling issues. This counter is cleared when the system is removed from power. The LEC-BW only monitors the board temperature and does not support TS#-Events.

Exception Blink Codes

In the case of an error, the BMC shows a blink code on the STATUS-LED (LED1). This error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash storage and is cleared when the power is removed. Therefore, the “Clear Exception Code”-Command is not supported.

Table 4-41: Blink Codes

Exception Blink Code	Error Message
0	NOERROR
2	NO_SUSCLK
3	NO_SLP_S5
4	NO_SLP_S3
5	RESET_FAIL

Table 4-41: Blink Codes (Continued)

6	
7	POWER_FAIL
8	LOW_VIN
9	NO_PWRGD_ATX
10	NO_PWRGD_1V0S
11	NO_PWRGD_1V2S
13	NO_PWRGD_1V8S
14	NO_PWRGD_3V3S
15	NO_PWRGD_1V5S

BMC Flags

The BMC Flags register returns the last detected exception code since power up.

4.3 Watchdog Timer

The LEC-BW features three separate Watchdog Timers. One of them is integrated in the SoC and two are provided by the BMC (managed by the SEMA).

The SoC Watchdog can be configured in the BIOS or by programming the Watchdog registers. If this function is used by user application, the application has to provide all logging functionality if desired.

The BMC Watchdog activations are caused by under voltage protection. The Watchdog LED flashes after restart but only if the power supply reaches 4.2V.

4.4 Temperature Sensors

The LEC-BW supports two temperature sensor functions. One is offered from the SoC and one from a dedicated chip (Texas Instruments LM73) on the board.

The SoC temperature sensors can be configured by programming the appropriate SoC registers. Refer to the Thermal Management chapter in the N-series Intel processor data sheet for more information. The on-board LM73 temperature sensor is managed by the BMC and is configured through the SEMA utility.

4.5 Programming Examples

Programming examples can be provided based on a Linux operating system, upon request.

Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in Table A-1 below. Requests for support through Ask an Expert are given the highest priorities, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the ADLINK web site at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called “My ADLINK”, unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the My Question area where you can check status, update your request, and access other features.
- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1: Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	**ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110 San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

Table A-1: Technical Support Contact Information (Continued)

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1 Shang Di East Rd.
Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8626
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园
A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

LiPPERT ADLINK Technology GmbH
Address: Hans-Thoma-Strasse 11
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Email: emea@adlinktech.com

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KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
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